Altitude and Underground Real-Time SER Characterization of CMOS 65 nm SRAM

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***Abstract*—We report real-time SER characterization of CMOS 65 nm SRAM memories in both altitude and underground environments. Neutron and alpha-particle SERs are compared with data obtained from accelerated tests and values previously measured for CMOS 130 nm technology.**

***Index Terms*—Accelerated tests, alpha contamination, atmospheric neutrons, neutron-induced SER, real-time testing, SER simulation, single-Event Rate (SER), static memory, terrestrial radiation environment.**

I. Introduction

With the constant downscaling of CMOS technologies, the susceptibility of integrated circuits to radiation coming from the natural terrestrial environment (primarily atmospheric neutrons) or induced by on-chip radioactive impurities (source of alpha particles) has been recognized as one of the highest failure rates of all reliability concerns, including for example electro-migration, gate rupture or Negative Bias Thermal Instabilities (NBTI) [1]–[3]. Current ultra-scaled memory ICs have been found to be more sensitive to Single Event/Single Bit Upset (SEU/SBU) and especially to Multiple Bit/Multiple Cell Upset (MBU/MCU) [4], [5]. This sensitivity is a direct consequence of the reduction of device dimensions and spacing within memory cells combined with the reduction of supply voltage and node capacitance, resulting in a decrease of both the critical charge (i.e., the minimum amount of charge required to induce the flipping of the logic state) and the sensitive area (i.e., the minimum collection area inside which a given particle can deposit enough charge to induce the flipping of the cell) [5]–[9]. Because the response and sensitivity of a given technology to cosmic rays or (internal) residual radioactivity have not necessary the same magnitude (depending on several design and process key-parameters, such as the 3D cell architecture, the circuit layout and the internal contamination level of chip materials and package), its impact on the soft-error rate (SER) must be separately evaluated in terms of fail occurrence (SEU/SBU and MCU/MBU aspects) and failure-in-time (FIT) for both neutrons and alpha-particles [11].

In the continuation of recent works dedicated to the real-time testing of a CMOS 130 nm bulk SRAM technology [12]–[14], this new study precisely deals with the measurement of neutron and alpha induced SER in state-of-the-art 65 nm SRAMs from long-term experiments performed both in altitude (on the Altitude SEE Test European Platform—ASTEP) and underground (at the Modane Underground Laboratory—LSM). The altitude location was chosen to strengthen natural neutron irradiation; the cave environment allows to completely screen the atmospheric neutron contribution and to quantify the remaining alpha SER directly induced by the presence of radioactive impurities in the chip materials. In the following, we briefly describe the devices under test, hardware setup, test procedure (Section II) and test environments (Section III) before detailing our real-time results (Section IV) and comparing the data with values separately obtained by accelerated test. Data analysis and comparison with failure rates previously measured for CMOS 130 nm technology will be finally reported and discussed in the last section (Section V).

II. Experimental Details

A. Device Under Test

Real-time measurements have been currently performed on bulk SRAMs fabricated by STMicroelectronics using a commercial CMOS 65 nm Low Power (LP) technology process. This process is based on a Boro-Phospho-Silicate Glass (BPSG)-free Back-End Of Line (BEOL) which eliminates the major source of $^{10}\mathrm{B}$ in the circuits; and drastically the possible interaction between $^{10}\mathrm{B}$ and low energy neutrons (in the thermal range and below) [15]–[17].

The circuit is a test vehicle (chip PROMO65, 25 mm^2, 75 millions of transistors) developed for library qualification and process monitoring. It contains 8.5 Mb of Single Port SRAM (SP-SRAM, bit cell area of 0.525 $\mu\mathrm{m}^2$) and 1.0 Mb of Dual Port

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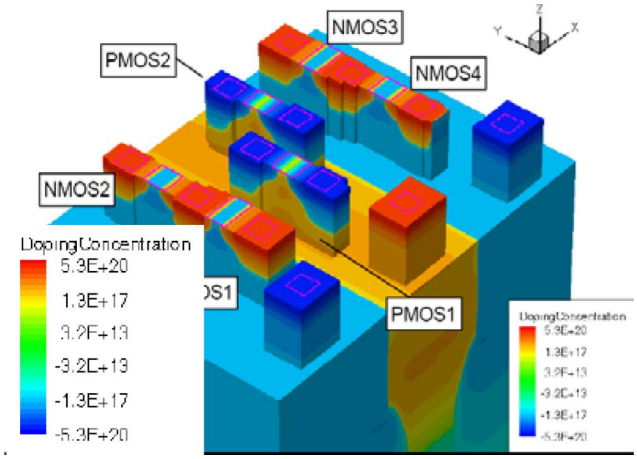

Fig. 1. Full 3-D structure of the bulk 65 nm SP-SRAM (6 transistors, bit cell area of 0.525 μm^2). STI structures have been removed for better showing Silicon regions below transistor active area. The simulation domain contains more than 300,000 mesh elements.

SRAM (DP-SRAM, bit cell area of 0.98 μm^2). The SP-SRAM bitcell, shown in Fig. 1, corresponds to the standard 6 transistors SRAM designed with one access transistor on each internal node. DP-SRAM has the same electrical schematic with two additional access transistors, one on each side of the memory, giving the ability to simultaneously read and write different memory cells at different addresses.

Both SP-SRAM (Fig. 1) and DP-SRAM bitcells were fully modeled with 3D TCAD tools (included in the version 10.0 of Sentaurus Synopsys package [18]) to evaluate their sensitivity to heavy ions and to determine the SEU/SBU and MBU/MCU occurrences as a function of ion parameter [7], [9].

In complement to TCAD work, numerous experimental studies were conducted these two last years to characterize the PROMO65 chip from an accelerated-test point-of-view with neutrons at the Los Alamos Neutron Science Center (LANSCE), as well as with an intense Am^{241} alpha source at STMicroelectronics.

B. Hardware Setup

Two identical SER test equipments (one per test site), specially designed for the study, have been developed and assembled by iRoC Technologies [19]. Fig. 2 shows a general view of the test equipment. In the present configuration, each system is capable of monitoring 384 chips and performing all requested operations such as writing/reading data to the chips, comparing the output data to the written data and recording details on the different detected errors in both embedded SP-SRAM and DP-SRAM parts of the PROMO65 chips.

The technical solution uses a PC to monitor a single rack of DUT boards through a dedicated SER tester. The tester is in charge of test setup drive and test algorithm execution. Computer is used to pilot and to collect data logged in the tester. The different hardware and software components have been designed to strictly follow all the specifications of the JEDEC Standard JESD89A [11]. In particular, the design of the setup ensures that all detected errors come from the devices under test,

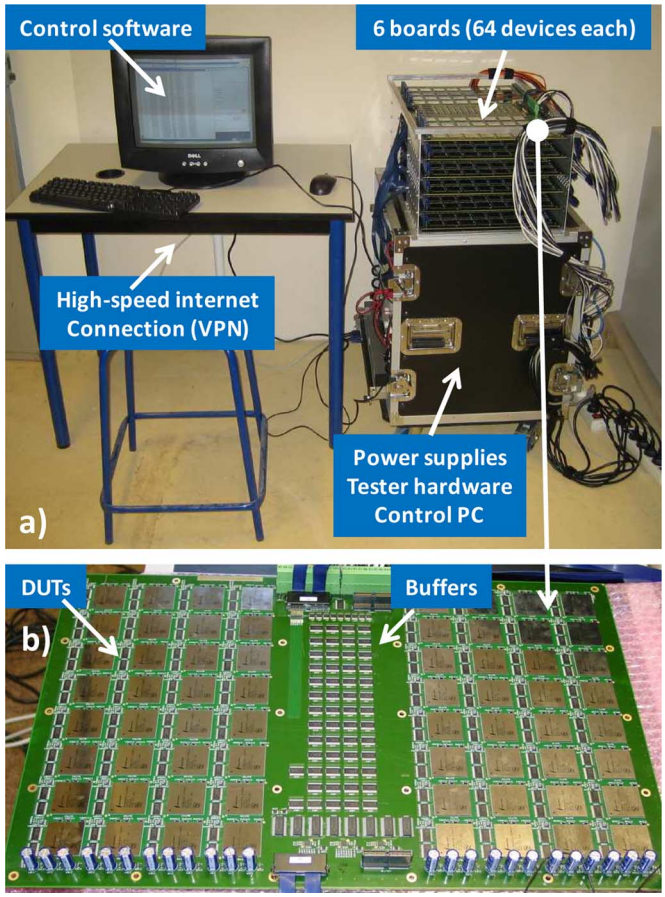

Fig. 2. a) General view of the SRAM automatic test equipment (here photographed on the ASTEP platform) and b) detail of one motherboard. The system is designed to test 384 chips dispatched on 6 motherboards. Chips (directly connected on motherboards) are horizontally oriented during the test. The system deployed at LSM is strictly identical for both hardware and software aspects.

not from external or system noise, by respecting the following guidelines [15], [19]:

1) The test operation is such that once a failing data is detected, the data is read again a given number of times before data is rewritten. Consistency of failed data over these read cycles ensures that the failure is a soft error in the DUT.
2) The tester implements high reliability system techniques: redundancy in the logic interface with the DUT and watch-dog for periodic re-initialization of the tester.
3) The power supplies are designed for uninterruptible operation and very low noise. The power supply voltages are permanently monitored. The voltage and current drawn by the DUT during the standby mode are logged periodically.
4) The DUT boards are properly designed for very low internal noise. The boards are multi-layered with alternated signal and ground planes for high immunity to EMI. They are also designed with controlled impedance for maintaining signal integrity with a relatively high number of circuits in a bus. The DUT chips are connected in daisy-chain with a limited number of chips in each bus (Fig. 2). An FPGA is controlling the read and write operations for each DUT board.

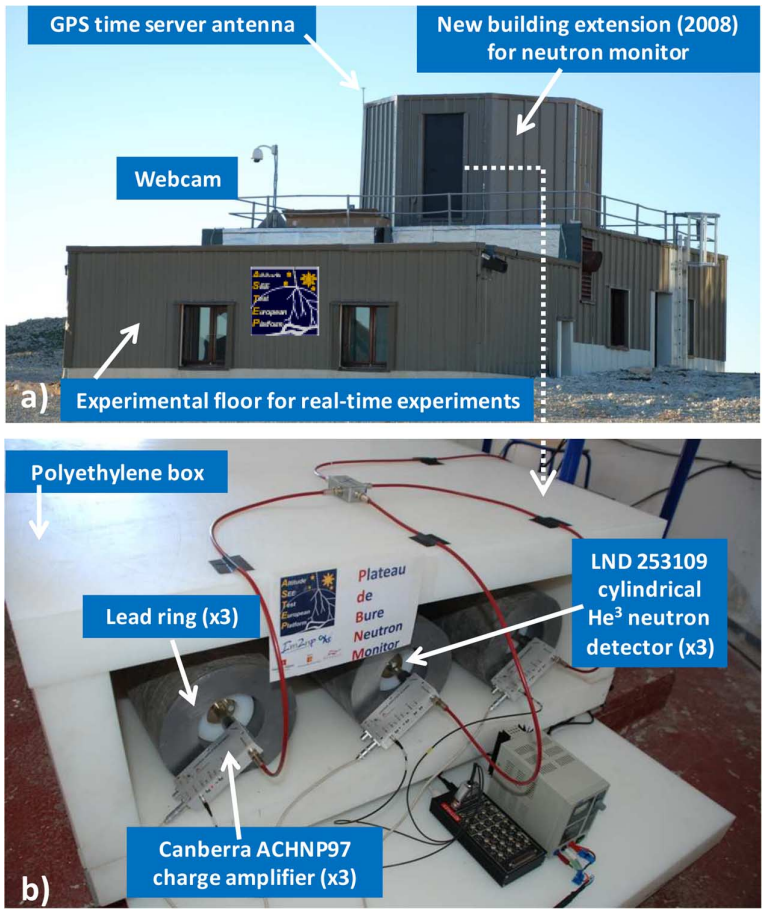

Fig. 3. a) External view ASTEP building showing the new extension (first floor) designed to host the Plateau de Bure Neutron Monitor (PdBNM). b) View of the extremities of the cylindrical neutron detector tubes connected to the charge amplifiers and to the acquisition module (electronic counters).

5) Finally, the tester and array of DUT boards are properly shielded against EMI.

C. Test Strategy Details

The test of PROMO65 devices is based on dynamic tests (permanent accesses) to all devices. At power on, all devices are written with the reference pattern; then all devices are read back in loop to check for errors. The read operation duration for the 384 devices is 2.5 seconds. The test algorithm used for this dynamic testing, allows detection of SBU, MCU, Single-Event Failure Interrupt (SEFI) or Single-Event Latchup (SEL) events. Current consumption of all power lines provided by the tester is monitored and logged during the test. User can see in real time the errors on the monitor of the tester. This test algorithm has dead time, but with the considered conditions of real-time SER (very low error rate), it is negligible.

III. Test Platforms and Environments

Real-time SER test equipments were deployed on the two test locations, i.e., on the ASTEP platform and at LSM, during the first semester of 2008. In the following, we very briefly give a few details about these two host laboratories.

A. The ASTEP Platform

ASTEP is a dual academic research and R&D platform (permanent facility) founded by STMicroelectronics, JB R&D and L2MP-CNRS in 2004 [12]. The current platform, operated by IM2NP-CNRS (formerly L2MP), is dedicated to real-time SER testing of semiconductor circuits and systems. Located in the French Alps on the desert Plateau de Bure at 2552 m, in a low electromagnetic noise environment, the platform is hosted by the Institute for Radio-astronomy at Millimeter Wavelengths

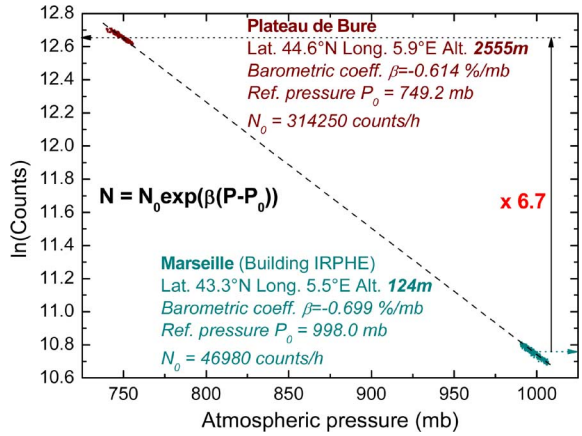

Fig. 4. Experimental determination of the ASTEP acceleration factor (AF) from the barometric response of the neutron monitor successively installed in Marseille (2007–2008) and on the Plateau de Bure since July 2008. Experimental clouds correspond to one month recording (one point per hour).

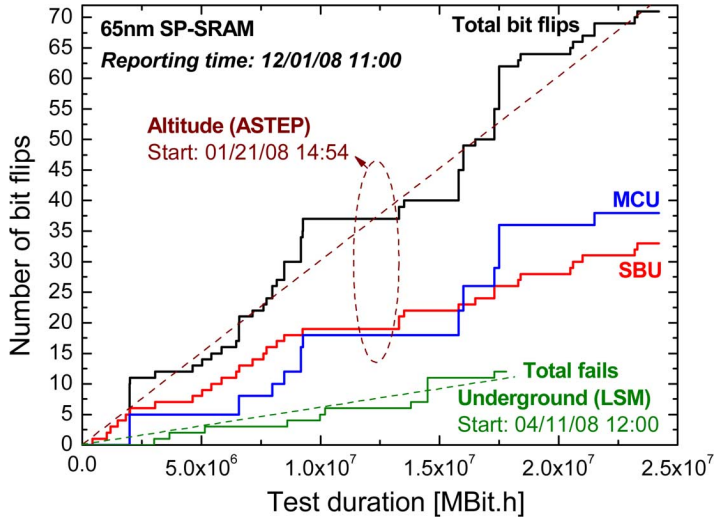

Fig. 5. Cumulative total fails, SBU and MCU flips versus test duration for the 65 nm SP-SRAM during both altitude and underground experiments. Test has been conducted under nominal conditions: $V_{\mathrm{DD}} = 1.2\ \mathrm{V}$, room temperature, standard checkerboard test pattern.

(IRAM). ASTEP is fully operational since March 2006: it is referenced in the JEDEC standard JESD89A as a research location [11]. Main environment characteristics of the ASTEP platform can be found in [12].

Since July 2008 and in complement to SER testing facilities, ASTEP has been now providing in situ real-time neutron monitoring using a super 3-NM64 neutron monitor installed in a new extension of the ASTEP building (Fig. 3). The Plateau de Bure Neutron Monitor (PdBNM) is composed of three high pressure (2280 Torr) cylindrical He^3 detectors surrounded by lead rings and a polyethylene box. The design and the construction of the PdBNM followed the recommendations published in [20], [21] for the optimization of the apparatus response. Assembled and previously operated in Marseille during the year 2007–2008, the PdBNM was transported and installed on the Plateau de Bure in July 2008. This gave us the unique opportunity to experimentally determine the acceleration factor (AF) of the ASTEP location with strictly the same setup. Fig. 4 shows the barometric response of the PdBNM, i.e., the variation of the counting rate as a function of the atmospheric pressure [22]. The difference between the counting rates of the two clouds of experimental points (~ 700 hourly data, which corresponds to one month monitoring) directly gives the value of the acceleration factor of ASTEP with respect to Marseille location, here estimated to 6.7. Taking into account latitude, longitude and altitude corrections for Marseille location with respect to the reference one, i.e., New-York City, the final value of the acceleration factor is $\mathrm{AF} = 6.7 \times 0.94 \approx 6.3$. This value is close to 6.2, the average acceleration factor reported in the Annex A of the JEDEC standard JESD89A [11], [23], and close to 5.9, the value given by the Qinetic Radiation Atmospheric Model (QARM) [24], [25]. In the following, we will use the experimental value $\mathrm{AF} = 6.3$ as the acceleration factor for the ASTEP location.

In complement to this important indication, the PdBNM will be use in future work to follow in parallel the time evolution of the neutron flux (average value depending of the neutron monitor response function [B-C]) and the cumulative distribution of fails observed in microelectronic circuits.

B. *The Underground Laboratory of Modane (LSM)*

The underground laboratory of Modane is located about 1700 m under the top of the Fréjus mountain (4800 meters water equivalent), near the middle of the Fréjus highway tunnel connecting France and Italy [26]. It was created in 1983 in order to conduct particle physics and astrophysics experiments in a strongly reduced cosmic ray background environment. Due to the depth of the LSM, the average particle flux inside the laboratory is extremely reduced:

- $4\ \mathrm{muons/m^2/day}$ corresponding to a two million reduction factor compared to the flux at sea level;
- 3×10^3 fast $\mathrm{neutrons/m^2/day}$ (in the energy range 2–6 MeV) emitted by natural radioactivity from the rock, the neutron component of cosmic rays being totally eliminated at this depth.

In addition, the Radon in the laboratory is maintained at a very low rate of $\sim 20\ \mathrm{Bq/m^3}$ owing to an air purification system which totally renews the volume of the air inside the laboratory twice an hour.

Recent fast neutrons measurements performed by E. Yakushev at immediate proximity of our setups give an upper limit of fast neutron flux $\approx 4 \times 10^{-6}\ \mathrm{neutron/cm^2/s}$, confirming the residual background value of only a few 10^3 fast $\mathrm{neutrons/m^2/day}$ inside the experimental room [27].

IV. Experimental Results

This section is dedicated to our experimental results obtained for the 65 nm technology from real-time (i.e., life-testing) and accelerated tests (for both neutrons and alphas) on chips PROMO65 (SRAM test vehicle). In the following, all numerical results have been normalized by a common arbitrary scaling factor, set lower than 3 ×. The real order of magnitude for the reported data is thus not significantly altered.

A. *Real-Time Measurements*

Fig. 5 shows the cumulative number of fails detected in SP-SRAMs versus test duration (expressed in $\mathrm{MBit} \times \mathrm{h}$) for

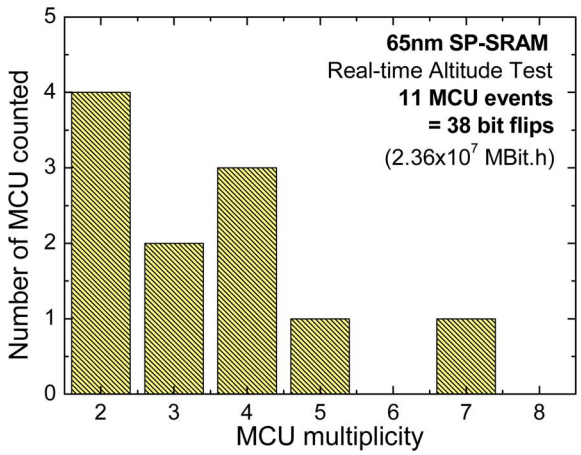

Fig. 6. Distribution of the MCU multiplicity (i.e., number of bit flips per MCU event) for the 11 MCU events detected during the altitude test (SP-SRAM). These MCUs involves a total of 38 bit flips which correspond to physical adjacent bit cells (in the memory plan) in all cases.

both altitude and cave experiments. Because the two experiments started at different dates, the number of $\mathrm{MBit} \times \mathrm{h}$ cumulated in altitude ($2.42 \times 10^7\ \mathrm{MBit} \times \mathrm{h}$) is higher than the value reached in the cave experiment ($1.78 \times 10^7\ \mathrm{MBit} \times \mathrm{h}$). A data analysis summarized in Table I shows that for the altitude experiment a total of 44 events (involving a total of 71 bit flips) was detected for SP-SRAM, including 33 SBU and 11 MCU. These MCUs involves a total of 38 bit flips which are physical adjacent bit cells in all cases with a multiplicity ranging from 2 to 7. The distribution of these MCUs is given in Fig. 6. Note that this MCU contribution represents $11/44 = 25\%$ of the detected events and $38/71 = 53.5\%$ of the total number of detected bit flips, confirming via a real-time experiment the importance of MCU mechanisms in such a deep submicron technology. For the cave experiment, only 12 fails were recorded, corresponding to 10 SBU and 1 MCU (involving 2 adjacent cells). The fraction of MCU is reduced in this case to 16.7% of the total number of detected bit flips. Experimental data consistency (i.e., compliant with a "random process") was checked for the altitude experiment (the number of bit flips is statistically representative) in terms of statistical distribution of $0 \rightarrow 1$ and $1 \rightarrow 0$ bit flips and error bitmap: the frequency of bit flips is found close to 50% for each transition which are randomly distributed in the memory plan.

From data of Fig. 5 for both experiments, we estimated the real-time SER at the test location, reported in Table I, using the following expression:

$$\mathrm{SER} = \frac{N_r}{\Sigma_r} \times 10^9 \left(\frac{\mathrm{FIT}}{\mathrm{MBit}}\right) \tag{1}$$

where N_r is the number of bit flips (for flip SER), SBU (for SBU SER) or MCU events (for MCU SER) observed at time T_r and Σ_r is the number of $\mathrm{MBit} \times \mathrm{h}$ cumulated at time T_r.

We also reported in Table I the upper and lower confidence intervals at 90% level based on the $\div^2$ distribution in order to estimate the experimental error margins [11]. We verified

TABLE I
SUMMARY AND KEY-VALUES FOR THE REAL-TIME 65 NM EXPERIMENT

ALTITUDE EXPERIMENT	SP-SRAM	DP-SRAM
Starting date	01/21/08 14:54	
Reporting date	12/01/08 11:00	
Cumulated number of Mbit.h	2.42×10^7	2.84×10^6
Total number of events/bit flips	44/71	8/10
Number of SBU	33	6
Number of MCU/MCU flips	11/38	2/2
SBU SER on ASTEP (FIT/Mbit)	1364	2113
MCU SER on ASTEP (FIT/Mbit)	455	704
Total flip SER on ASTEP (FIT/MBit)	**2934**	**3521**
Lower and upper confidence limits for the total flip SER (FIT/Mbit)	*2423* *3574*	*2172* *5973*

UNDERGROUND EXPERIMENT		
Starting date	04/11/08 12:00	
Reporting date	12/01/08 11:00	
Cumulated number of Mbit.h	1.78×10^7	2.10×10^6
Total number of events/bit flips	11/12	2/2
Number of SBU	10	2
Number of MCU/MCU flips	1/2	0/0
SBU SER (FIT/Mbit)	562	952
MCU SER (FIT/Mbit)	56	0
Total flip SER (FIT/Mbit)	**674**	**952**
Lower and upper confidence limits for the total flip SER (FIT/Mbit)	*432* *1092*	*389* *2998*

that the convergence of SER vs. test hours is asymptotically reached within ~ 3000 h of experiment (which corresponds to $\sim 10^7\ \mathrm{Mbit} \times \mathrm{h}$). Beyond this duration, the total flip SER remains constant around 2934 FIT/Mbit for the altitude experiment and around 674 FIT/Mbit for the underground test.

The calculation of the normalized neutron real-time SER at the reference location of New-York City (NYC) is obtained from the following expression, assuming that the fail rate due to alpha-particles is identical to the alpha-SER experimentally deduced from underground experiment:

$$\begin{cases} \text{neutron-SER}|_{NYC} = \frac{\mathrm{SER}|_{ASTEP} - \mathrm{SER}|_{LSM}}{AF} \\ \text{alpha-SER}|_{NYC} = \mathrm{SER}|_{LSM} \end{cases}. \tag{2}$$

In (2), the value of the acceleration factor of the ASTEP site is taken equal to $\mathrm{AF} = 6.3$, the experimental value determined from data collected using the Plateau de Bure neutron monitor. The normalized neutron-SER is then equal to $(2934 - 674)/6.3 = 359\ \mathrm{FIT/MBit}$ and the total flip SER for both alpha and neutron contributions is equal to $359 + 674 = 1033\ \mathrm{FIT/MBit}$ for the 65 nm SP-SRAM.

For DP-SRAM and because the test circuit only contains 1 MBit per chip (against 8.5 Mbit for SP-SRAM), the statistics is not yet totally satisfactory, as illustrated by the very large confidence interval reported in Table I. Therefore, a first estimation gives for the altitude test a value of $\sim 3521\ \mathrm{FIT/Mbit}$ and $\sim 952\ \mathrm{FIT/Mbit}$ for the cave experiments, resulting in normalized (NYC) $\mathrm{neutron\text{-}SER} = 407\ \mathrm{FIT/MBit}$. SER values for DP-SRAM will be consolidated in a future work. In the following, we will only consider results related to SP-SRAM for comparison with 130 nm and discussion.

TABLE II
SUMMARY OF FLIP SER VALUES ($\mathrm{Normalized}^*$) OBTAINED FROM ACCELERATED TESTS ($V_{\mathrm{DD}} = 1.2$ V, ROOM TEMPERATURE, STANDARD CHECKERBOARD TEST PATTERN)

		SP-SRAM	DP-SRAM
Alpha-SER (FIT/Mbit)	**Total flip SER**	**605**	**798**
Neutron-SER (FIT/MBit)	SBU SER	353	461
	MCU (event) SER	38	21
	Total flip SER	**470**	**535**

Extrapolated to 0.001 alpha/cm²/h and 13 neutrons/cm²/h.

B. Accelerated Test

Table II report results of neutron and alpha accelerated test results performed on 65 nm chips. The test procedures were fully compliant with the JEDEC test standard JESD89A [11].

Alpha-SER was evaluated from accelerated measurements using an intense Am^{241} alpha source. The tests were performed in a characterization lab at Crolles2. The alpha source is a thin foil of Am^{241} which has an active diameter of 1.1 cm. The source activity was 3.7 MBq, as measured on the 1st February 2002. The alpha particle flux was precisely measured in March 2003 with a Si detector which was placed at 1 mm from the source surface. This calibration measurement gave an alpha flux of 1.05×10^6 $\mathrm{alpha/cm^2/s}$. Since the atomic half-life of Am^{241} is 432 years, the activity and flux values recalculated for each experimental session are still very accurate. The reported SER values have been extrapolated to a nominal alpha flux of 0.001 $\mathrm{alpha/cm^2/h}$. This value emulates the alpha emissivity rate for the semi-conductor processing and packaging materials with an "ultra low alpha" grade. During the SER experiments, the Americium source lies above the chip package. Therefore, the distance source-die is minimum and approximately equal to 1 mm (same distance as for the calibration). All experiments were performed at room temperature (25°C). Experimental measurements (Table II) led to an accelerated $\mathrm{alpha\text{-}SER} = 605$ FIT/Mbit for SP-SRAM and 790 FIT/Mbit for DP-SRAM.

Accelerated neutron-SER evaluation has been conducted at the LANSCE WNR facility, at Los Alamos (USA) in August 2006. The neutron flux available at LANSCE during the experiment was 1.6×10^5 $\mathrm{n/cm^2/sec}$, which is 40% of the LANSCE maximum flux (this is a limitation at LANSCE facility for the whole year 2006). The beam is collimated and uniform over a ~ 8 cm diameter. The neutron fluence was measured by LANSCE uranium fission chamber. The total number of produced neutron is obtained by counting fissions and applying a proportionality coefficient. The reported SER values, shown in Table II, have been extrapolated to the reference (NYC) neutron integrated flux of 13 $\mathrm{neutrons/cm^2/h}$: we obtained 470 FIT/Mbit and 535 FIT/Mbit, for SP-SRAM DP-SRAM, respectively. The MCU contribution represents $\sim 31\%$ of the total detected events in these accelerated tests.

V. DATA ANALYSIS AND DISCUSSION

In this last section, we analyze and discuss real-time data reported in Section IV. We also report for comparison experimental data related to another ST technology (130 nm SRAM) previously characterized in another study [14]. Additional results deduced from accelerated SER tests and from wafer-level measurements are finally presented.

A. Real-Time Versus Accelerated Tests for 65 nm

The direct comparison of real-time and accelerated SER values, reported in Section IV.A for 65 nm SP-SRAMs, shows a very reasonably agreement between the two sets of data, especially for alpha-SER: we measured 674 FIT/MBit (real-time) and 605 (accelerated) FIT/MBit for alpha-SER, resulting in a difference of only 11%, typically within the experimental error margins; we also measured 359 FIT/Mbit (real-time) and 470 FIT/Mbit (accelerated) for neutron-SER, showing in this case an agreement within 30% margins. This very good agreement observed for the alpha-SER tests firstly suggests that the accelerated alpha-emission setup was properly designed and the test operation accurately conducted. In addition, the real-time SER value suggests that the alpha-emission rate for the semiconductor processing and packaging materials is very close to the value of 0.001 $\mathrm{alpha/cm^2/h}$ initially assumed to calculate the accelerated SER value reported in Table II.

For neutron-SER, a discrepancy of 30% between the two approaches remains very acceptable with respect to dosimetry errors and/or statistical dispersions from sample-to-sample, lot-to-lot and error intervals on the knowledge of some physical, technological and electrical key-parameters (manufacturing variability) [15], [28]. Moreover, this result could be explained by possible differences between the neutron-beam and the real atmospheric neutron spectra, largely introduced by the cut-off energy of the accelerator which is always well below cosmic ray energies. This could be also confirmed by the relatively important difference in the percentages of bit flips involved in MCU events for the two experiments: 53.5% for real-time and 31% for accelerated tests.

Our recent results concerning heavy ion testing and 3D simulations of MCU occurrence in 65 nm SRAMs [9] are coherent with this observation: the contribution of MCU to the total number of upsets strongly increases with the LET of the incident ion, suggesting that high energy neutrons (indirectly inducing a non negligible fraction of high LET ions) play a major role in the occurrence of large size MCUs effectively observed in real-time experiments. This MCU aspect will be consolidated in a future work, by more increasing the experiment duration to significantly improve the statistics on MCUs (Fig. 6).

B. 65 nm Versus 130 nm Technologies

In this paragraph, we compare data related to the 65 nm technology with real-time measurements of another STMicroelectronics 130 nm technology previously extensively characterized in dedicated studies [14]. The test vehicle for the 130 nm technology is composed of 4 MBit SP-SRAM with a bit cell area of 2.50 $\mu\mathrm{m}^2$. A total of 3,664 MBit was considered for real-time experiments, both in altitude (ASTEP) and underground (LSM). Real-time data have been collected with strictly the same setup in both locations; this setup was successively installed on ASTEP during the period [March 31, 2006–November 6, 2006] and then transported to the LSM and

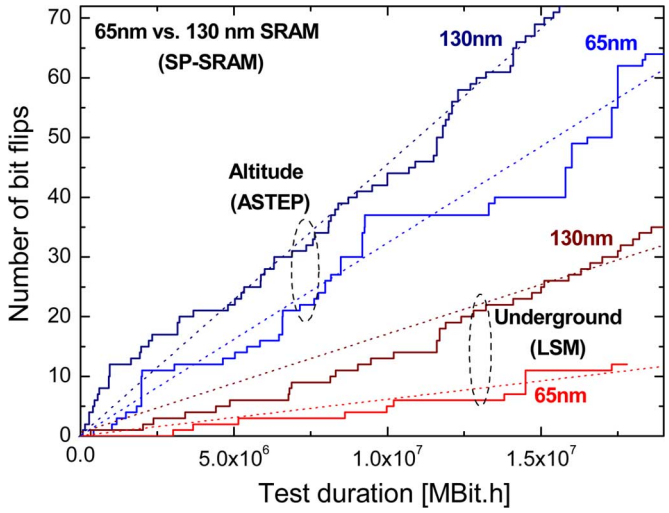

Fig. 7. Cumulative total fails versus test duration for both 130 nm and 65 nm SP-SRAMs detected in altitude and underground. Test has been conducted under nominal conditions for both technologies: $V_{DD} = 1.2$ V, room temperature, standard checkerboard test pattern. For 130 nm data, experiment periods are [March 31, 2006–November 6, 2006] for the altitude test and [October 16, 2007–November 24, 2008] for the underground test.

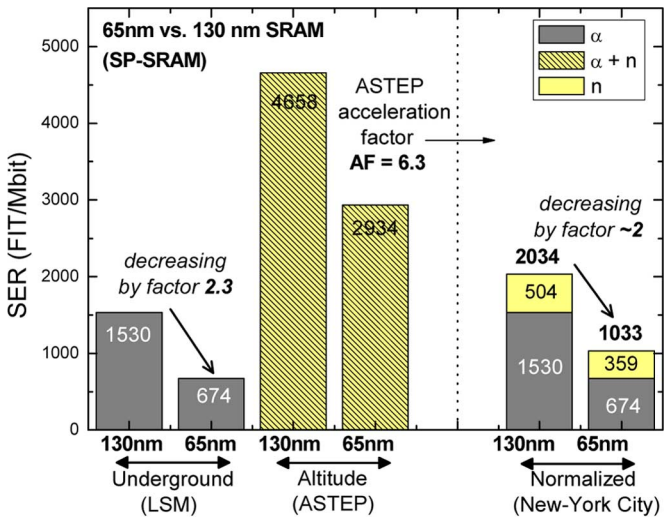

Fig. 8. Synthesis of experimental real-time SER values obtained for both 130 nm and 65 nm SP-SRAM from altitude and underground experiments and normalization of the SER at the reference flux of New-York City (sea-level) [4] taking into account i) the alpha contribution for the altitude test (fixed to the value measured at LSM) and ii) the ASTEP acceleration factor $\mathrm{AF} = 6.3$ for the neutron flux in altitude (experimentally measured using the Plateau de Bure Neutron Monitor).

running during the period [October 16, 2007–November 24, 2008].

Fig. 7 shows a direct comparison of the total bit flip distributions versus test duration for the two technologies. For the 130 nm, a total of 72 bit flips was detected after 1.55×10^7 MBit$\times$h in altitude, 35 fails after 1.9×10^7 MBit$\times$h during the underground test. The analysis of Fig. 7 indicates that, for both test locations, the 130 nm technology exhibits a higher soft-error rate (directly linked to the slope of the curves) than the 65 nm one.

In addition, for the altitude test, 5 MCU events, involving each 2 physical adjacent bit cells, were recorded; no MCU event was detected for the cave experiment. This difference in MCU occurrence for the two technologies is clearly highlighted by the "staircase shape" of the curves: the 130 nm distribution has very regular stairs (each stair corresponding to a single bit flip), at the opposite, the 65 nm curve (especially for the altitude test) exhibits irregular and marked stairs, which is the "visual signature" of MCU events.

These SER values related to the 130 nm technology are reported in Fig. 8. We used (2) to separate alpha from neutron contributions to the total normalized SER value. Fig. 8 also summarizes the key-values of experimental real-time SER for both 130 and 65 nm technologies (SP-SRAM). Alpha-SER is found to decrease by a factor 2.3 for the 65 nm technology with respect to the 130 nm one and neutron-SER by a factor 1.4, resulting in a net improvement of the total SER by a factor ~ 2.

C. Estimation of the Alpha-Particle Emission Rates For 65 nm and 130 nm Technologies

Combining real-time and accelerated alpha-SER values, for a given technology, allows us to estimate the alpha-particle emission rate for the semiconductor processing and packaging materials. Because accelerated values are extrapolated (i.e., normalized) to the reference value of 0.001 $\mathrm{alpha/cm^2/h}$ (that corresponds to an "ultra low alpha" grade [2]), the real alpha-particle emission rate is simply given by this value multiplied by a factor corresponding to the ratio of the real-time SER by the accelerated SER. We thus obtain for the 65 nm technology $0.001 \times (674/605) \approx 1.1 \times 10^{-3}$ $\mathrm{alpha/cm^2/h}$. For the 130 nm technology, a similar calculation from real-time SER value given in Fig. 8 and considering the accelerated value of 380 FIT/Mbit reported in [14], we obtain: $0.001 \times (380/1530) \approx 4.0 \times 10^{-3}$ $\mathrm{alpha/cm^2/h}$.

In addition to this indirect extraction of the alpha-particle emissivity via SER tests, the alpha emission rates for both the tested wafers and packages (mold compound) were accurately characterized using an ultra-low alpha background counter (gas flow type). The tests were performed in a characterization lab at Crolles2. A high purity in terms of radioactive contaminants was confirmed, around $(0.9 \pm 0.3) \times 10^{-3}$ $\mathrm{alpha/cm^2/h}$ for the 65 nm technology. In parallel, the same measurement procedure was applied for the characterization of wafers and packages of the 130 nm technology. A value of $(2.3 \pm 0.2) \times 10^{-3}$ $\mathrm{alpha/cm^2/h}$ was obtained, confirming with the same order of magnitude the reduction of the alpha-emitter contamination for the 65 nm technology with respect to the 130 nm one. The discrepancy between SER-based and direct counting measurements is small and very acceptable with respect to the experimental uncertainties for the alpha counting, the SER testing and the sample-to-sample/lot-to-lot variations for the trace amounts of alpha contaminants.

D. Synthesis and SER Trends

In this last paragraph, we would like to summarize in Table III all the values related to the two technologies characterized in the framework of this study. We also indicate in the last column of Table III the evolution factor between the 130 nm and 65 nm technologies. On one hand, a simple scaling of the sensitive area

TABLE III
65 NM VERSUS 130 NM TECHNOLOGIES (SINGLE-PORT SRAM): SYNTHESIS OF KEY-VALUES FOR REAL-TIME AND ACCELERATED TESTS

		130nm (SP)	65nm (SP)	130→65nm variation
Bit cell area (μm^2)		2.50	0.525	÷4.76
Sensitive volume (μm^3) [28]		0.025	0.0035	÷7.14
Critical charge (fC) [28]		2.5	0.8	÷3.13
Nominal V_{DD} (V)		1.2	1.2	unchanged
EXPERIMENTAL RESULTS				
Accelerated SER (FIT/Mbit)	Alphas	380*	605*	×1.6
	Neutrons	665*	470*	÷1.4
	Total	**1045**	**1075**	~unchanged
Real-time SER (FIT/Mbit)	Alphas	1530	674	÷2.27
	Neutrons	504	359	÷1.4
	Total	**2034**	**1033**	**÷ ~2**
Alpha-particle emission level measured at wafer level (alphas/cm²/h)		(2.3±0.2) $\times 10^{-3}$	(0.9±0.3) $\times 10^{-3}$	÷2.5
Alpha-particle emission level deduced by combining accelerated and real-time data (alphas/cm²/h)		4×10^{-3}	1.1×10^{-3}	÷3.6

(*) Extrapolated to 0.001 alpha/cm²/h and 13 neutrons/cm²/h.

of the 130 nm SRAM versus the 65 nm SRAM should produce approximately a $\div 4$ reduction factor in the FIT/Mbit rates. On the other hand, as the cell size decreases, it holds less charge causing the critical charge to decrease, typically by a factor ~ 3 [29]. This makes it easier for the cell to be upset due a neutron-induced or an alpha particle strike. Since we only observe (from real-time data) a global $\div 2$ reduction factor, one could attribute this reduction to a combination of these two opposite trends, resulting in the sensitive area change with a small increase in the sensitivity of the basic cell [30]. The fact that the reduction factor is experimentally found (life-testing) more important for alpha-SER $(\div 2.27)$ than for neutrons $(\div 1.4)$ could be explained by the additional impact of the alpha-particle emission rate (decreasing by a factor at least > 2.5) on this scaling factor. Because such an impact is relatively complex to quantify on the final SER value characterizing a given technology, the in-depth analysis of the SER evolution from the 130 nm to the 65 nm technologies should require a specific dedicated work (including material-level and technological options, memory cell and circuits layout considerations [30]) that goes far beyond the present study.

VI. CONCLUSION

In summary, this study provides a complete set of original data obtained from real-time altitude and underground measurements on a state-of-the-art (65 nm) CMOS technology. By comparing accelerated and real-time measurements, it is noteworthy that for alpha particles both measurements are extremely close. This confirms that the alpha emission rate from the dice (wafer + package) is extremely close to the so-called "ultra low alpha" extrapolated level, corresponding the value of $0.001\ \mathrm{alpha/cm^2/h}$. For neutrons, accelerated and real-time measurements are as well in good agreement $(\sim 30\%)$ with respect to error margins in such experimental approaches. Data also shows and quantifies via a real-time experiment in natural environment the importance of MCU mechanisms in such a deep submicron technology. Direct comparison with real time measurements in 130 nm technology, tested in the same locations with a similar setup, clearly shows that the reduction of the neutron SER is related to the technologies (same trend than that of accelerated measurements) while for alpha it is related to a more complex evolution, combining the two opposite trends given by the technology (sensitive area, critical charge) with the observed decrease in the alpha emission rate for the semiconductor processing and packaging materials (trend opposite to that of accelerated measurements extrapolated to a given emission rate value).

In parallel to this characterization work, the installation of a neutron monitor on the altitude site (ASTEP) allowed us to precisely determine the acceleration factor related to the neutron flux and to validate previous results obtained for the 130 nm technology [9]–[12]. This neutron monitor will be use in future work to follow in parallel the time evolution of the neutron flux and the time distribution of fails observed in microelectronic circuits.

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