Device Reliability Report

Second Quarter 2014

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/07/2014	10.1	Changed many tables to show second quarter 2014 test data. Chapter 1, The Reliability Program Updated Table 1-16 and Table 1-17. Updated SEU and Soft Error Rate Measurements, page 26. Chapter 2, Results by Product Family Data was updated in many tables. The Autoclave Test section was removed for CPLDs. HASTU has substituted Autoclave for the reliability monitor program. Chapter 3, Results by Package Type Added packages for PQ160, PQ208, page 72 and FBG484, page 79.
05/02/2014	10.0	Changed many tables to show first quarter 2014 test data. Removed obsolete 0.22 µm Virtex® FPGA product data. Added package data for CLG400, FLG1926, FLG1928, and HCG1932. In Chapter 3, removed tables for packages CS280, CS484, FF1513, FF1517, PQ100, PQ160, PQ208, PQ240, CSG280, and PCG84. Added data for packages CLG400, FLG1926, FLG1928, and HCG1932. Added *Appendix A, Additional Resources and Legal Notices*.
03/18/2014	9.8	Replaced reliability data for package FFG1928, page 100. Added reliability data for package FLG1925, page 101. Revised the Revision History section for readability.
02/14/2014	9.7	Changed many tables to show fourth quarter, 2013 test data. Removed reliability data for the obsolete XCSxxxXL 0.25 µm device. Removed Spartan®-3 FPGA Autoclave data. HASTU has substituted Autoclave for the reliability monitor program. Chapter 1, The Reliability Program Updated Table 1-8 Product ESD and Latch-up Data, Table 1-15 ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs, Table 1-16 Summary of the Failure Rates, and Table 1-17 Real Time Soft Error Rates. Chapter 2, Results by Product Family Updated and moved existing tables. Updated test results in Temperature Cycling Test, page 41, High Accelerated Stress Test, page 46, Unbiased High Accelerated Stress Test, page 47, High Temperature Storage Life, page 50 and Unbiased High Accelerated Stress Test, page 57. Updated test results in Temperature Cycling Test, page 62, Unbiased High Accelerated Stress Test, page 63, and Data Retention Bake Test, page 65. Chapter 3, Results by Package Type Alphabetized Non-Hermetic packages SO20, VO20, VO48, PC44, PC84, PC20, PQ100, PQ160, PQ208, PQ240, TQ100, TQ144, VQ44, VQ100, HQ208, and HQ240. Removed package BGG256 from Reliability Data for Pb-Free Packages, page 77.

Date	Version	Revision
11/19/2013	9.6	Changed many tables to show third quarter, 2013 test data. Removed reliability data for the obsolete XC95xxx 0.5 µm device. Removed Spartan-3 FPGA Autoclave data. HASTU has substituted Autoclave for the reliability monitor program. Chapter 1, The Reliability Program Updated Table 1-7,Wafer Process Technology Family, Table 1-8, Product ESD and Latch-up Data, Table 1-15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs, Table 1-16, Summary of the Failure Rates, and Table 1-17, Real Time Soft Error Rates. Added devices XC7V2000T, XC7VH580T, XC7VX1140T, and XC7Z100 to Table 1-15. Chapter 2, Results by Product Family Deleted the Autoclave Test section in Temperature Cycling Test, page 41. Chapter 3, Results by Package Type Added packages BG352, BG432, BG560, page 67, FB676, page 68, FF484, FF784, page 68, FG320, page 70, FF896, FF900, FF901, page 69, BGG256, page 85, FBG900, page 79, FFG1513, FFG1517, page 81, FFG1696, FFG1704, FFG1738, FFG1759, FFG1760, FFG1761, page 81, FGG256, page 82, FLG1925, FLG1926, FLG1928, page 84, and FSG48, page 84. Added FBG900, SBG484, FFG1928 and their plots to Board-Level Reliability Tests, Pb-Free, page 95.

Date	Version	Revision
08/16/2013	9.5	Changed many tables to show second quarter, 2013 test data. Removed reliability data for the following obsolete devices: XC17(S)xxx/XL/E 0.6 µm XC4xxx/LE 0.5 µm XC4xxxE 0.5 µm XC4xxxXL 0.35 µm XCSxxx 0.35 µm XC4xxxXLA 0.25 µm XC95xxxXV 0.25 µm Chapter 1, The Reliability Program Updated Table 1-7,Wafer Process Technology Family, Table 1-8, Product ESD and Latch-up Data, Table 1-9, ESD and Latch-up Data for XC2VPxxx, Table 1-16, Summary of the Failure Rates, and Table 1-17, Real Time Soft Error Rates. Added XC7VX980T to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs. Chapter 2, Results by Product Family Deleted tables for obsolete devices. Updated data in many tables. Added Table 2-31, THB Test Results for Si Gate CMOS Device Type XC3SxxxA and Table 2-97, THB Test Results of Si Gate CMOS Device Type XC17SxxxA. Chapter 3, Results by Package Type Deleted these tables: Table 3-24, Tests of Package Type DD8 Table 3-25, Tests of Package Type Chip Scale CC44 Table 3-61, Test Results of Device Types XC7VX485T, XC7VX690T under heading FFG1927. Deleted PG132 and PG175 from Table 3-27, Tests of Package Types PG84, PG120, PG156, PG191, PG223, PG299, and PG475. Deleted CB-100 and CB164 from and added CB196 to Table 3-28, Tests of Package Types CB196 and CB228. Updated data in many tables. Added package CS484, page 73. Added packages FF1924, FF1926, FF1927, FF1928, FF1929, and FF1930, page 70. Added packages FFG1924, FFG1926, FFG1926, FFG1927, FFG1928, and FFG1930, page 81.

Date	Version	Revision
05/13/2013	9.4	Changed many tables to show first quarter, 2013 test data. Chapter 1, The Reliability Program Added 7 series devices XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T and Zynq-7000 AP SoC devices XC7Z010, XC7Z030, and XC7Z045 to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs. Updated data for 0.25 µm, 0.35 µm, and 0.5 µm process technologies in Table 1-16, Summary of the Failure Rates. Updated data for 40 nm, 45 nm, and 28 nm technology nodes in Table 1-17, Real Time Soft Error Rates. Chapter 2, Results by Product Family Data in many tables was updated. Removed duplicate Table 2-17, HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx. Deleted Table 2-69, Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxxXLA. Added Table 2-67, Temperature Cycling Test Results for Si Gate CMOS Device Type XCE4VxXxxx. Chapter 3, Results by Package Type Data in many tables was updated. Added packages FFG1923, FFG1924, FFG1925, FFG1926, FFG1927, FFG1928, FFG1929, FFG1930 and FFG1927 and their test results.
04/02/2013	9.3	Changed many tables to show fourth quarter, 2012 test data. Added Xilinx 7 series FPGAs and Zynq-7000 All Programmable SoCs. Chapter 1, The Reliability Program Added XC7A100T, XC7A200T, XC7K70T, and XC7Z020 devices to Table 1-15 ESD and Latch-up Data for 7 Series FPGAs. Failure rate data changed in Table 1-16 Summary of the Failure Rates. Text and data changed in SEU and Soft Error Rate Measurements, page 26. Chapter 2, Results by Product Family Data in many tables was updated. Added Table 2-33 THB Test Results for Si Gate CMOS Device Type XCVxxx, Table 2-35 THB Test Results for Si Gate CMOS Device Type XC2Vxxx, Table 2-32 THB Test Results for Si Gate CMOS Device Type XC2SxxxE, Table 2-81 HAST Test Results for Si Gate CMOS Device Type XC4xxxE, and Table 2-104 HASTU Test Results for Si Gate CMOS Device Type XC4xxxXLA. Deleted Table 2-167, Summary of the Test Results for device XC2Cxxx/A from The TH test is conducted under the conditions of 85°C and 85% RH. Package preconditioning is performed on the testing samples prior to the TH test., page 61. Chapter 3, Results by Package Type Data in many tables was updated. Added packages CS144, CS324, CLG400, CLG484, FFG323, FFG324, FFG363 and their respective test results in Table 3-9 Test Results for Device Types XCV50, XC2V80, Table 3-11 Test Results for Device Types XC6SLX45, XC6SLX45T, Table 3-29 Test Results for Device Types XC2V1000, XC2V1500, and Table 3-49 Test Results of Device Types XC5VLX50. Note: Table numbers are accurate as of the version 9.3 printing.

Date	Version	Revision
02/12/2013	9.2	Changed many tables to show the third quarter, 2012 test data. Added Xilinx 7 series FPGAs. Chapter 1, The Reliability Program Added XC7K160T, XC7K410T, XC7K420T, XC7K480T, XC7V585T, and XC7VX485T devices to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs. Chapter 2, Results by Product Family Added Table 2-34, THB Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-95, HAST Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-103, HASTU Test Results for Si Gate CMOS Device Type XC4xxxE, Table 2-110, HASTU Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-111, HASTU Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink), Table 2-120, HASTU Test Results for Si Gate CMOS Device Type XCE4VxXxxx, Table 2-125, High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4xxxXLA, Table 2-126, High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCSxxx, Table 2-141, High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCE4VxXxxx, and Table 2-160, Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P. Chapter 3, Results by Package Type Added packages FF665, FF672, FF676, FFG665, FFG672, and FFG896. Added Table 3-47, Test Results of Device Types XC5VLX30T and Table 3-56, Test Results of Device Type XC2V1000. Note: Table numbers are accurate as of the version 9.2 printing.

Date	Version	Revision
08/22/2012	9.1	Changed many tables to show the second quarter, 2012 test data. Chapter 1, The Reliability Program Added entries for devices XC6SLX4 and XC6SLX9. Removed obsolete reliability data for devices XC4VSX25, XC4VSX55, and XCV600E. Chapter 2, Results by Product Family Added entries for devices XC17S150A, XC3S250E, XC6VLX195T, XC7K410T, XC7VX485T, and XC9536. Removed obsolete reliability data for the following devices: XC17(S)xxx, XC17(S)xxx(X)L, XC17(S)xxxE, XC1702L, XC17S15A, XC17S200A, XC17S50XL, XC17Sxxx, XC17SxxxA, XC17SxxxXL, XC17Vxxx, XC18V01, XC18V02, XC18V04, XC18V512, XC18Vxxx, XC2C64, XC2S100E, XC2S150E, XC2V1500, XC2V3000, XC2VP100, XC2VP70, XC2VPxxx, XC2Vxxx, XC3S1000, XC3S100E, XC3S1400AN, XC3S200A, XC3SD1800A, XC3SDxxxA, XC3SxxxA, XC3SxxxAN, XC4013XLA, XC4VLX15, XC4VLX200, XC4VLX80, XC4VSX25, XC4VSX55, XC4xxxXLA, XC5VLX50T, XC6SLX150T, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX760, XC95144XL, XC95144XV, XC95288XV, XC95xxxXL, XC95xxxXV, XCF01S, XCF04S, XCF08P, XCF16P, XCF32P, XCFxxx, XCFxxxP, XCFxxxS, XCS20, XCS40XL, XCSxxx, XCSxxxXL, XCV1000E, XCV1600E, XCV400, XCV400E, XCV405E, XCV600E, XCV812E, XCVxxx (shrink), XCVxxxE, XCVxxxE (shrink) Chapter 3, Results by Package Type Added entries for devices XC7K410T and XC7VX485T. Removed obsolete reliability data for the following devices: XC17256E, XC17S100A, XC17S100XL, XC17S200A, XC17S50A, XC18V01, XC2C128, XC2C256, XC2S300E, XC2V1000, XC2V250, XC2V500, XC2V6000, XC2V80, XC2VP100, XC2VP50, XC2VP70, XC3S1500, XC3S4000, XC3S5000, XC4085XLA, XC4VLX100, XC4VLX25, XC5215, XC5VLX50, XC6SLX150T, XC6SLX16, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX240T, XC6VLX475T, XC6VLX760, XCE2VP50, XCF01S, XCF02S, XCF04S, XCF08P, XCF16P, XCF32P, XCR3064XL, XCS40XL, XCV1000E (shrink), XCV1600E, XCV2000E, XCV2000E (shrink), XCV300E (shrink), XCV600, XCV600E
05/08/2012	9.0	Changed many tables to show the first quarter, 2012 test data. Added Xilinx 7 series FPGAs.
01/27/2012	8.1	Updated Chapter 1, The Reliability Program Added XCE6VxXxxx to Table 1-7. Added XC5VSX240T to Table 1-12. Chapter 2, Results by Product Family Added XCE6VxXxxx to Table 2-1. Deleted XC2S150 from Table 2-8. Added XCV100 to Table 2-9. Added XC6SLX45 and XC6SLX100 to and deleted XC6SLX16 from Table 2-23. Added XC4VLX160 and XC4VFX12 and modified Note 1 in Table 2-24. Added Note 1 to Table 2-25 and Table 2-26. Inserted new table: Table 2-29. Added XC5VLX85T to table Table 2-45. Added XC6VLX365T to Table 2-46. Added XCS20XL to and deleted XCS10XL from Table 2-71. Added XC3S200AN to Table 2-84. Added XC6SLX4 to Table 2-85. Added XC2S100E to and deleted XC2S400E from Table 2-93. Added XCS20XL and XCSxxxX to Table 2-105. Added XC6SLX4 and XC6SLX9 to Table 2-117. Deleted XCR3064XL from Table 2-178. Added XC2C64 to Table 2-194. Added XCR3128XL to Table 2-214. Added XC2C64 to Table 2-215. Chapter 3, Results by Package Type Added HTS to Table 3-3 and Table 3-47. Added HAST to Table 3-56. Note: Table numbers are accurate as of the version 8.1 printing.

Date	Version	Revision
11/07/2011	8.0	Changed most tables to show the third quarter, 2011 test data. Chapter 1, The Reliability Program Updated Acceptance Criteria and added note 3 to Table 1-3. Chapter 2, Results by Product Family Added XCV600E to Table 2-12. Added XC2VP7 to and deleted XC2VP80 from Table 2-15. Deleted XC3S2000 from Table 2-18. Deleted XC4VLX15 from Table 2-24. Added XC6VLX130T to Table 2-28. Added XC4VLX80 to Table 2-43. Added XC2V6000 to Table 2-77. Deleted XC4VFX100 and XC4VLX85T from Table 2-85. Added XC5VLX330T device to Table 2-86. Added XC6VLX195T device to Table 2-87. Added XC6SLX25T to Table 2-99. Added XCV100 to Table 2-123. Added XC6SLX16 to Table 2-136. Added XC4VLX80 to Table 2-137. Deleted XC17S150XL from Table 2-146. Deleted XCF128X from Table 2-148. Deleted XC17S30XL from Table 2-152. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-155. Deleted XC17S30XL from Table 2-163. Deleted XC17V16 from Table 2-164. Deleted XC17S30XL from Table 2-169. Deleted XC17V16 from Table 2-170. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-172. Deleted XC95216 from Table 2-174. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-192. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-201. Added XCR3256XL and deleted XCR3128XL XCR3512XL from Table 2-213. Chapter 3, Results by Package Type Added HASTU to Table 3-11. Deleted HTS from Table 3-12. Deleted HASTU from Table 3-15. Deleted Temperature cycling –40 to +125°C row from Table 3-26. Added HASTU to Table 3-29. Added HTS to Table 3-43. Added HAST to Table 3-47. Added Temperature cycling -55 to +125°C row and HTS to Table 3-49. Added HTS to Table 3-66. Added Temperature humidity 85°C, 85% RH with bias row to Table 3-74. Note: Table numbers are accurate as of the version 8.0 printing.
08/02/2011	7.0	Changed most tables to show the **second** quarter, 2011 test data.
06/17/2011	6.0.1	Revised last sentence in SEU and Soft Error Rate Measurements, page 26 for clarity.
05/09/2011	6.0	Changed most tables to show the first quarter, 2011 test data.
02/01/2011	5.12	Changed most tables to show the fourth quarter, 2010 test data.
11/01/2010	5.11	Changed most tables to show the third quarter, 2010 test data.
08/10/2010	5.10	Changed most tables to show the second quarter, 2010 test data.
05/04/2010	5.9	Changed most tables to show the first quarter, 2010 test data.
03/15/2010	5.8	Changed most tables to show the fourth quarter, 2009 test data.
10/27/2009	5.7	Updated most tables to include third quarter, 2009 test data. Added alpha particle FIT/Mb data for Spartan®-6 and Virtex®-6 FPGAs to Table 1-14, page 19. Note: Table number is accurate as of the version 5.7 printing.
08/03/2009	5.6	Changed most tables to show the second quarter, 2009 test data.
06/15/2009	5.5	Added SF363 (Lot 2) data to Table 3-62, page 102. Replaced Figure 3-1, page 103, Figure 3-2, page 103, and Figure 3-3, page 104. Revised FFG1704 data in Table 3-64, page 108. Note: Table and Figure numbers are accurate as of the version 5.5 printing.

Date	Version	Revision
05/07/2009	5.4	Changed most tables to show the first quarter, 2009 test data. Added second paragraph to SEU and Soft Error Rate Measurements, page 26.
02/11/2009	5.3	Changed most tables to show the fourth quarter test data. Added single event upset and soft error rate data. See Table 1-14, page 19. Note: Table number is accurate as of the version 5.3 printing.
11/14/2008	5.2	Changed most tables to show the third quarter test data. Updated legal disclaimer.
08/15/2008	5.1	Changed most tables to show the second quarter test data.
07/07/2008	5.0	Changed most tables to show the first quarter test data.
02/06/2008	4.3	Changed most tables to show the fourth quarter test data.
10/31/2007	4.2	Changed most tables to show the third quarter test data.
09/18/2007	4.1.1	Corrected omission in this history table.
08/24/2007	4.1	Changed most tables to show the second quarter test data.
06/04/2007	4.0	Changed most tables to show the first quarter test data.
03/28/2007	3.3.2	Corrected typos in four tables.
02/20/2007	3.3.1	Corrected typos in three tables.
02/12/2007	3.3	Changed most tables to show the fourth quarter test data.
12/01/2006	3.2	Changed most tables to show the third quarter test data.
10/06/2006	3.1.2	Corrected values in tables 1-12, 2-87, 2-90, and 2-91.
08/29/2006	3.1.1	Changed typos in tables 2-91, 3-44, and 3-55.
08/11/2006	3.1	Changed most tables to show the second quarter test data.
06/20/2006	3.0.1	Corrected two transposed figures in Table 1-10.
05/05/2006	3.0	Changed most tables to show the first quarter test data.
02/24/2006	2.9	Updated most tables to reflect the fourth quarter test data.
11/17/2005	2.8	Updated most tables to include the third quarter test data.
08/19/2005	2.7	Changed most tables to show the second quarter test values.
05/20/2005	2.6	Corrected data in tables 2-61 and 3-32.
03/01/2005	2.5	Changed most tables to show the fourth quarter test values. Removed packaging information from Chapter 1 and added a reference to the packaging website.
01/04/2005	2.4	Added third quarter data.
08/18/2004	2.3	Added second quarter data.
05/24/2004	2.2	Changed Tables 1-1, 2-1, 2-15, 3-44, 3-46, 3-48, 3-50, 3-52 and a heading on page 75.
05/24/2004	2.1	Changed fit rate on page 7 for 0.5 µm from 89 to 8.
05/10/2004	2.0	First quarter 2004 revision.
02/09/2004	1.0	Initial release in new template.

Table of Contents

Chapter 3: Results by Package Type

Appendix A: Additional Resources and Legal Notices

The Reliability Program

Overview

Xilinx publishes this report to provide customers with insight regarding the reliability of Xilinx® products. Reliability is defined as product performance to specification over time in response to varied (specified) environmental stress conditions. The goal of the reliability program is to achieve continuous improvement in the robustness of each product being evaluated.

As part of this program, finished product reliability is measured periodically to ensure that the product performance meets or exceeds reliability specifications. Reliability programs are executed in response to internal programs.

The reliability qualifications of new devices, wafer processes, and packages are designed to ensure that Xilinx products satisfy internal requirements before transfer into production. The reliability qualification and monitoring requirements are outlined in Table 1-1 through Table 1-16. The reliability stress tests are conducted according to the conditions specified in JEDEC Solid State Technology Association' s reliability test methods for packaged devices, JESD22, except Group B and D tests in which it follows DSCC test methods, MIL-STD-883.

Product Qualification

The reliability tests used for wafer process qualification are summarized in Table 1-1.

Table 1-1: **Wafer Process Qualification Tests**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
High-temperature operating life (HTOL)	$T_J \geq 125°C$, V_{DD} Max	1,000 hours	3	77	200 FIT(1) 50 FIT(2)
THB(3) or High-accelerated stress test (HAST)(3)	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			

Table 1-1: **Wafer Process Qualification Tests *(Cont'd)***

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
Temperature humidity (TH)[3] or Unbiased high accelerated stress test (HASTU)[3]	85°C, 85% RH	1,000 hours	3	25	0 failures
	130°C, 85% RH	96 hours			
	110°C, 85% RH	264 hours			
Temperature cycling (TC)[3][4][5][6]	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to+125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Data Retention Bake[7] or High Temperature Storage (HTS)	T_A = 150°C	1,000 hours	3	25	0 failures
Program Erase[8]	T_A = 25°C	10,000 cycles	1	32	0 failures

Notes:

1. Phase I production is released as the qualification data demonstrates, meeting the required 200 FIT failure rate and other test requirements.
2. Phase II production is released as the qualification data demonstrates, meeting the required 50 FIT failure rate and other test requirements.
3. Package preconditioning is performed prior to THB, HAST, temperature cycling, TH, and HASTU tests.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.
5. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
6. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
7. For CPLD and EPROM products.
8. This is not a mandatory test and only for CPLD and EPROM products.

Non-Hermetic and Hermetic Packages

Moisture sensitivity and reflow temperature information can be found in *Device Package User Guide* (UG112) [Ref 1].

The non-hermetic package/assembly qualification is outlined in Table 1-2. However, for hermetic package qualification, a full group B and D test per MIL-STD-833, *Test Methods*, is required.

Table 1-2: **Non-Hermetic Package/Assembly Qualification**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB[1] or HAST[1]	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			

Table 1-2: **Non-Hermetic Package/Assembly Qualification *(Cont'd)***

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
Temperature cycling(1) (2)(3),(4)	–65°C to +150°C	500 cycles,	3	25	0 failures
	–55°C to +125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Autoclave(1) or temperature humidity unbiased(1) or HASTU(1)	121°C, 100% RH	96 hours	3	25	0 failures
	85°C, 85% RH	1,000 hours			
	130°C, 85% RH or 110°C, 85% RH	96 hours or 264 hours			
High-Temperature Storage (HTS)	T_A=150°C	1,000 hours	3	25	0 failures

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
3. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.

The qualification process for new devices is shown in Table 1-3.

Table 1-3: **Device Qualification**

Reliability Test	Conditions	Lot Quantity	Sample Size per Lot	Target Criteria
ESD	HBM(1)	1	3	1,000V
ESD	CDM(2)	1	3	250V(3)
Latch-up	Current injection	1	3	200 mA

Notes:

1. HBM = Human Body Model.
2. CDM = Charge Device Model.
3. GT transceiver CDM level is specified per JEP157.

Reliability Monitor Program

The wafer process reliability monitor program is based on the maturity of the wafer process, the number of device hours, and the FIT rate. All processes are divided into one of two classes to determine how often the process is monitored annually. Class 1 processes are monitored every quarter; Class 2 processes are monitored every other quarter. FIT Rate calculations for both classes are based on approximately one million device hours (at T_J = 125°C) per fab if the data is available. Processes that are four years old or less are monitored every quarter regardless of the FIT rate. Mature processes older than four years

are monitored based on the FIT Rate. Table 1-4 summarizes the classification criteria and monitoring frequency for both classes.

Table 1-4: **Monitoring Process Classes**

	Class 1	Class 2
Classification Criteria	Process Age ≤ 4 years or FIT > 26 (for FPGAs), 55 (for Flash PROM)	Process Age > 4 years and FIT < 26 (for FPGAs), 55 for Flash PROMs)
Monitor Frequency	4 times per year	2 times per year

The reliability tests used to monitor the wafer process are shown in Table 1-5.

Table 1-5: **Tests Used to Monitor Wafer Processes**

Reliability Test	Condition	Duration	Lot Quantity	Sample Size per Process per Family per Quarter
HTOL	T_j > 125°C, V_{DD} Max	1,000 hours	1	45
Data Retention Bake(1)	T_A = 150°C	1,000 hours	1	45

Notes:

1. For CPLD and PROM products.

The package reliability monitor program takes into consideration the following factors:

- Package construction (wire-bond lead frame, wire-bond BGA, or flip chip)
- Factory location (assembly site, or wafer fabrication site)
- Substrate vendor
- Die size
- Technology maturity
- Past history

Based on these factors and availability, representative packages are drawn from inventory for the stress tests defined in Table 1-6. These tests are typically conducted on a quarterly basis, but the number of tests can be reduced or eliminated based on the maturity of the package technology, understanding of failure mechanisms, and their dependency on the stress test.

Table 1-6: **Tests Used by the Reliability Package Monitor Program**

Reliability Test	Stress Conditions	Stress Duration	Sample Size	Frequency
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hrs	45	WBLF(2) every even quarter WBBGA(3) every odd quarter Flip Chip (4) every quarter
	130°C, 85% RH, V_{DD}	96 hrs		
	110°C, 85% RH, V_{DD}	264 hrs		
Temperature cycling(1)(5)	–55°C to +125°C or –40°C to +125°C	1,000 cycles	45	WBLF every quarter WBBGA every quarter Flip Chip every quarter
Autoclave(1)(5) or Temperature humidity unbiased(1)(5) or HASTU(1)(5)	121°C, 100% RH	96 hrs	45	WBLF every odd quarter WBBGA every even quarter
	85°C, 85% RH	1,000 hrs		
	130°C, 85% RH or 110°C, 85% RH	96 hrs or 264 hrs		
HTS(7)	T_A=150°C	1,000 hrs	45	WBLF every quarter WBBGA every quarter

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For matured WBLF packages (PLCCs, SOICs, and DIPs packages), reliability monitoring is performed once a year.
3. For matured WBBGA packages (S-BGA Cavity-down BGA), reliability monitoring is performed once a year.
4. For flip chip packages, THB testing is performed every quarter and replaces the need for temperature humidity testing.
5. For plastic QFP and BGA packages: –55°C to +125°C and 1,000 cycles; for flip chip packages: –55°C to +125°C and 1,000 cycles or 40°C/+125°C and 1,000 cycles.
6. Refer to the device-specific qualification report for complete autoclave, temperature humidity, and HASTU reliability test data.
7. HTS stress is not applicable with flip chip package because the technology has no wire-bond IMC interface degradation.

Process Technology Family

Table 1-7 lists the Xilinx devices that support various process technologies.

Table 1-7: **Wafer Process Technology Family**

Process Technology	Device
0.028 µm	7 series FPGAs and Zynq®-7000 All Programmable (AP) SoCs
0.040 µm	XC6VxXxxx, XCE6VxXxxx
0.045 µm	XC6Sxxx
0.065 µm	XC5VxXxxx, XCE5VxXxxx
0.09 µm	XC3Sxxx, XC3SxxxA, XC3SxxxAN, XC3SxxxE,XC3SDxxxA, XC4VxXxxx, XCE4VxXxxx
0.13 µm	XC2VPxxx, XCE2VPxxx
0.15 µm	XC2Vxxx, XCE2Vxxx

Table 1-7: **Wafer Process Technology Family *(Cont'd)***

Process Technology	Device
0.15 µm	XC18Vxxx, XCFxxxS/P
0.18 µm/ 0.15 µm	XCVxxxE (shrink), XC2SxxxE
0.18 µm	XCVxxxE, XC2Cxxx
0.22 µm/ 0.18 µm	XC2Sxxx, XCVxxx (shrink)
0.35 µm/ 0.25 µm	XC95xxxXL
0.35 µm	XCRxxxXL
0.35 µm	XC17SxxxA

ESD and Latch-up Summary

ESD results are obtained according to specifications ANSI/ESDA/JEDEC JS-001-2010 and JEDEC JESD22-C101. Latch-up results are obtained by using specification EIA/JESD78. ESD tests are performed at 25°C. In general, the latch-up data for newer products such as Zynq-7000 AP SoCs, 7 series, Virtex®-4, Virtex®-5, Virtex®-6, Spartan®-3, and Spartan®-6 devices are collected at 125°C unless specified otherwise.

ESD and latch-up data are summarized by family in these tables:

- Table 1-8: PROMs, CPLDs, and older FPGAs
- Table 1-9: Virtex-II Pro devices
- Table 1-10 and Table 1-11: Virtex-4 devices
- Table 1-12: Virtex-5 devices
- Table 1-13: Spartan-6 devices
- Table 1-14: Virtex-6 devices
- Table 1-15: 7 series FPGAs and Zynq-7000 AP SoCs

Table 1-8: **Product ESD and Latch-up Data**

Device	Latch-up	Human Body Model	Charge Device Model
XC18Vxxx/XCFxx	+200 mA	+2,000V	+500V(1)
XCVxxxE	+210 mA	+1,000V to +2,500V(4)	+300V(3)
XCVxxxE/XC2SxxxE	+210 mA	+2,000V to +3,000V	+500V(4)
XC2Sxxx	+210 mA	+2,000V	+500V(5)
XC95xxxXL	+200 mA	+2,000V to +3,000V	+1,000V(6)

Table 1-8: **Product ESD and Latch-up Data *(Cont'd)***

Device	Latch-up	Human Body Model	Charge Device Model
XCRxxxL	+200 mA	+2,000V to +3,000V	+500V(7)
XC2Vxxx	+200 mA	+750V to 2,000V(12)	+500V
XC2Cxxx	+200 mA	+2,000V	+500V
XC3Sxxx	+200 mA	+2,000V	+500V
XC3SxxxE	+200 mA	+2,000V	+500V
XC3SxxxA	+200 mA	+2,000V	+500V

Notes:

1. Measured on XC18V04 and XCF32P
2. Only XCV100E and XCV812E have ESD threshold below 2KV, (XCV100E passed at 1.5KV and XCV812E passed at 1KV)
3. Measured on XCV50E
4. Measured on XCV2600 (shrink)
5. Measured on XC2S200
6. Measured on XC9536XL
7. Measured on XCR3064XL
8. Human body model data collected on XC2V40, XC2V80, XC2V250, XC2V500, XC2V1000, XC2V1500, XC2V2000, XC2V3000, XC2V4000, XC2V6000, and XC2V8000
   Using the human body model, these devices have a threshold below 2KV: The XC2V40 passes at 1.75KV. The XC2V4000 (from UMC 8D) passes at 1.5KV. The XC2V500 pass at 750V.
   Results do not include DXN and DXP temperature sensing pins.
   Results do not include VBATT pins for XC2VxxxX devices.

The ESD results in Table 1-9 do not include DXN and DXP temperature sensing pins.

Table 1-9: **ESD and Latch-up Data for XC2VPxxx**

Device	Latch-up ±200 mA	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		Regular I/O and Power	MGT	Regular I/O and Power	MGT
XC2VP2	Pass	±1,500V	±2,000V	±500V	±300V
XC2VP4	Pass	±2,000V	±1,500V	±500V	±300V
XC2VP7	Pass	±2,000V	±1,000V	±500V	±500V
XC2VP20	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP30	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP40	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP50	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP70	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP100	Pass	±2,000V	±1,000V	±500V	±300V

Table 1-10: **ESD and Latch-up Data for XC4VFXxxx**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		STDIO	MGT	STDIO	MGT
XC4VFX12	Pass	±2,000V	N/A	±450V	N/A
XC4VFX60	Pass	±2,000V	±1,000V	±500V	±300V
XC4VFX40	Pass	±2,000V	±1,000V	±500V	±300V
XC4VFX20	Pass	±2,000V	±1,000V	±500V	±300V
XC4VFX100	Pass	±2,000V	±1,000V	±450V	±300V
XC4VFX140	Pass	±2,000V	±1,000V	±500V	±300V

Table 1-11: **ESD and Latch-up Data for XC4VLXxxx and XC4VSXxxx**

Device	Latch-up	Human Body Model Passing Voltage	Charge Device Mode Passing Voltage
XC4VLX15	Pass	±2,000V	±500V
XC4VLX25	Pass	±2,000V	±450V
XC4VLX40	Pass	±2,000V	±450V
XC4VLX60	Pass	±2,000V	±400V
XC4VLX80	Pass	±2,000V	±450V
XC4VLX100	Pass	±2,000V	±350V
XC4VLX160	Pass	±2,000V	±450V
XC4VLX200	Pass	±2,000V	±350V
XC4VSX25	Pass	±2,000V	±500V
XC4VSX35	Pass	±2,000V	±450V
XC4VSX55	Pass	±2,000V	±400V

Table 1-12: **ESD and Latch-up Data for XC5VxXxxx/T**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO(1)	GTP	SelectIO	GTP
XC5VLX20T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VLX30	Pass	±2,000V	N/A	±400V	N/A
XC5VLX30T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VLX50	Pass	±2,000V	N/A	±400V	N/A
XC5VLX50T	Pass	±2,000V	±1,000V	±400V	±250V(2)
XC5VLX85	Pass	±2,000V	N/A	±400V	N/A
XC5VLX85T	Pass	±2,000V	±1,000V	±400V	±250V(2)

Table 1-12: **ESD and Latch-up Data for XC5VxXxxx/T *(Cont'd)***

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO[1]	GTP	SelectIO	GTP
XC5VLX110	Pass	±2,000V	N/A	±400V[3]	N/A
XC5VLX110T	Pass	±2,000V	±1,000V	±400V[3]	±250V[2]
XC5VLX155	Pass	±2,000V	N/A	±400V	N/A
XC5VLX155T	Pass	±2,000V	±1,000V	±400V	±250V[4]
XC5VLX220	Pass[5]	±2,000V	N/A	±400V	N/A
XC5VLX220T	Pass[5]	±2,000V	±1,000V	±400V	±250V[4]
XC5VLX330	Pass[6]	±2,000V	N/A	±400V	N/A
XC5VLX330T	Pass[6]	±2,000V	±1,000V	±400V	±250V[2]
XC5VFX30T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX70T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX100T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX130T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VFX200T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VSX35T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VSX50T	Pass	±2,000V	±1,000V	±400V	±250V[2]
XC5VSX95T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VSX240T	Pass	±2,000V	±1,000V	±400V	±250V[2]
XC5VTX150T	Pass	±2,000V	±1,000V	±400V	±250V
XC5VTX240T	Pass	±2,000V	±1,000V	±400V	±250V

Notes:

1. Human body model passing voltage for VBATT pin is 1,000V. This data is updated based on the data collected after the HBM tester was upgraded to remove the HBM-ESD trailing pulse.
2. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, charge device model passing voltage is 200V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
3. Charge device model passing voltage for VBATT pin is 300V.
4. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, the CDM level is 150V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
5. The D_IN and CS_B pins on XC5VLX220 and XC5VLX220T devices pass at 150 mA.
6. The D_IN, CS_B, and RDWR_B pins on XC5VLX300 and XC5VLX330T devices pass at 150 mA.

Table 1-13: **ESD and Latch-up Data for XC6Sxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX4	Pass	±2,000V	N/A	±500V	N/A
XC6SLX9	Pass	±2,000V	N/A	±500V	N/A

Table 1-13: **ESD and Latch-up Data for XC6Sxxx *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX16	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX45	Pass	±2,000V	N/A	±500V	N/A
XC6SLX45T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX75	Pass	±2,000V	N/A	±500V	N/A
XC6SLX75T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX100	Pass	±2,000V	N/A	±500V	N/A
XC6SLX100T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX150	Pass	±2,000V	N/A	±500V	N/A
XC6SLX150T	Pass	±2,000V	±2,000V	±500V	±450V

Table 1-14: **ESD and Latch-up Data for XC6VxXxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC6VLX75T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX130T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX195T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX240T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX365T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX550T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX760	Pass	±2,000V(1)	N/A	±500V(2)	N/A
XC6VSX315T	Pass	±2,000V(1)	±1,000V	±500V(2)	±200V
XC6VSX475T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX250T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX255T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX380T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V

Table 1-14: **ESD and Latch-up Data for XC6VxXxxx *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC6VHX565T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V

Notes:

1. If the system monitor function is used, HBM passing voltage is: ±1,000V for all of the devices.
2. If the system monitor function is used, CDM passing voltage for the AVDD, AVSS, VN, VP, VREFN, VREFP, DXN and DXP pins is: ±200V for XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VSX315T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices; ±150V for XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380Tdevices. The DXN and DXP pins can withstand CDM voltages up to 500V without impacting the temperature sensing function.
3. The CDM passing voltage for the CCLK pin of the XC6VSX475T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices is 450V.

Table 1-15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7A35T	Pass	±2,000V	±1,500V	±350V	±300V
XC7A50T	Pass	±2,000V	±1,500V	±350V	±300V
XC7A75T	Pass	±2,000V	±1,500V	±350V	±300V
XC7A100T	Pass	±2,000V	±1,500V	±350V	±300V
XC7A200T	Pass	±2,000V	±1,500V	±350V	±250V
XC7K70T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K160T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K325T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K355T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K410T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K420T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K480T	Pass	±2,000V	±1,500V	±350V	±300V
XC7V585T	Pass	±2,000V	±1,500V	±350V	±250V
XC7V2000T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VH580T	Pass	±2,000V	±1,500V	±350V	±200V
XC7VH870T	Pass	±2,000V	±1,500V	±350V	±200V
XC7VX330T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX415T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX485T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX550T	Pass	±2,000V	±1,500V	±350V	±200V

Table 1-15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7VX690T	Pass	±2,000V	±1,500V	±350V	±200V
XC7VX980T	Pass	±2,000V	±1,500V	±350V	±200V
XC7VX1140T	Pass	±2,000V	±1,500V	±350V	±200V
XC7Z010	Pass	±2,000V	N/A	±350V	N/A
XC7Z015	Pass	±2,000V	±1,500V	±350V	±300V
XC7Z020	Pass	±2,000V	N/A	±350V	N/A
XC7Z030	Pass	±2,000V	±1,500V	±350V	±300V
XC7Z045	Pass	±2,000V	±1,500V	±350V	±300V
XC7Z100	Pass	±2,000V	±1,500V	±350V	±300V

Failure Rate Determination

The failure rate is typically defined in FIT units. One FIT equals 1 failure per 1 billion device hours. For example, 5 failures expected out of 1 million components operating for 1,000 hours have a failure rate of 5 FIT. The following is the failure rate calculation method:

$$\text{Failure Rate} = \frac{x^2 10^9}{2(\text{No. of Devices})(\text{No. of Hours})(\text{Acc. Factor})} \quad \text{Equation 1-1}$$

where:

x^2 = Chi-squared value at a desired confidence level and (2f + 2) degrees of freedom, where f is the number of failures.

The acceleration factor is calculated using the Arrhenius relationship:

$$A = \exp\left\{\frac{E_a}{k}\cdot\left(\frac{1}{T_{J1}} - \frac{1}{T_{J2}}\right)\right\} \quad \text{Equation 1-2}$$

where:

E_a = Thermal activation energy (0.7eV is assumed and used in failure rate calculation except EPROM in which 0.58 eV is used).

A = Acceleration factor

k = Boltzman's constant, 8.617164×10^{-5} eV/°K

T_{J1} = Use junction temperature in degrees Kelvin (°K = °C + 273.16)

T_{J2} = Stress junction temperature in degrees Kelvin (°K = °C + 273.16)

Failure Rate Summary

Table 1-16: **Summary of the Failure Rates**

Process Technology	Device Hours at TJ = 125°C	FIT(1)
0.028 µm	1,199,840	10
0.040 µm	1,526,588	8
0.045 µm	1,230,312	10
0.065 µm	3,238,316	8
0.09 µm	8,612,310	6
0.13 µm	2,247,240	5
0.15 µm (FPGA)	3,111,240	4
0.15 µm (EPROM)	2,110,352	12
0.18 µm/0.15 µm	2,480,031	10
0.18 µm	3,804,196	14
0.22 µm/0.18 µm	2,106,920	6
0.35 µm/0.25 µm	2,249,421	5
0.35 µm	1,076,451	11
0.35 µm (EPROM)	1,061,222	23

Notes:

1. FIT is calculated based on 0.7 eV (0.58 eV for EPROM), 60% C.L. and TJ of 55°C.

SEU and Soft Error Rate Measurements

Table 1-17 shows the soft error rates caused by single event upsets (SEUs) affecting memory cells used as configuration memory and block RAM. Neutron cross-sections are determined from LANSCE beam testing according to JESD89A/89-3A. Soft error rates (in FIT/Mb) are determined from real time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A. All data is current as of date of this report.

An upset in any configuration bit does not create a soft functional error per se. The bit has to be one that is critical to the function in order for a soft error to occur. The number of unused bits and non-critical bits reduces the soft error rate by what is known as the device vulnerability factor (DVF). The DVF for a typical design is 5% (one in 20 upsets, on average, cause a functional soft error). In the worst case, the DVF is never smaller than one in ten, or never worse than 10% of the upsets cause a soft functional error.

Xilinx offers a significant portfolio of SEU mitigation and analysis solutions that aid the developer to understand and interpret soft error rates and manage SEU rates in any given design. Consult your Xilinx sales and field support for assistance in understanding these capabilities, and visit our Single Event Upsets website for more background.

The actual SEU FIT rate of a design running in a Xilinx FPGA is far lower than what is predicted by direct calculation from the numbers in Table 1-17. This is because most FPGA routing resources are unused within any particular implementation.

Table 1-17: **Real Time Soft Error Rates**

Technology Node	Product Family	Neutron Cross-section per Bit[1]			FIT/Mb (Alpha Particle)[2]			FIT/Mb [6] (Real Time Soft Error Rate)[3]		
		Config. Memory	Block	Error	Config. Memory	Block RAM	Error[4]	Config. Memory	Block RAM	Error[4]
250 nm	Virtex	9.90×10^{-15}	9.90×10^{-15}	±18%				160	160	±20%
180 nm	Virtex-E	1.12×10^{-14}	1.12×10^{-14}	±18%				181	181	±20%
150 nm	Virtex-II	2.56×10^{-14}	2.64×10^{-14}	±18%				405	478	±8%
130 nm	Virtex-II Pro	2.74×10^{-14}	3.91×10^{-14}	±18%				437	770	±8%
90 nm	Virtex-4	1.55×10^{-14}	2.74×10^{-14}	±18%				263	484	±11%
90 nm	Spartan-3	2.40×10^{-14}	3.48×10^{-14}	±18%				190	373	–50% +80%
90 nm	Spartan-3E Spartan-3A	1.31×10^{-14}	2.73×10^{-14}	±18%				104	293	–80% +90%
65 nm	Virtex-5	6.70×10^{-15}	3.96×10^{-14}	±18%				165	692	–13% +15%
45 nm	Spartan-6	1.00×10^{-14}	2.20×10^{-14}	±18%	135	180	–50% +100%	188	395	–11% +12%
40 nm	Virtex-6	1.26×10^{-14}	1.14×10^{-14}	±18%	9	94	-48% +110%	106	251	-12% +14%
28 nm	7 series FPGAs	6.99×10^{-15}	6.32×10^{-15}	±18%	25	22	-64% +374%	83	75	-13% +15%

Notes:

1. Data from Los Alamos Neutron Science Center (LANSCE).
2. Spartan-6 FPGA alpha data based on thorium foil testing and package alpha emissivity of 0.0015 counts/cm^2/hr. Virtex-6 and 7 series FPGA alpha data estimated using real time underground cave testing.
3. Data compiled from the Rosetta experiment which includes upsets from neutron secondaries and packaging alpha particles. See *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits (*WP286) [Ref 2].
4. 90% confidence interval.
5. Configuration memory and block RAM memory utilization is reported by the ISE and Vivado tools. For accurate soft error failure rate estimation, consult the tool reports.
6. One FIT equals 1 failure per 1 billion device hours. Mb = 1e6 memory bits

Results by Product Family

FPGA Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD} and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

The failures listed in Table 2-1 are also listed in each family device table with failure analysis results in the footnotes.

Table 2-1: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2Sxxx	10	0	446	896,821	1,025,372	11
XCVxxx (shrink)	12	0	486	959,922	1,081,545	11
XCVxxxE	31	3	1,240	1,768,713	2,741,592	20
XCVxxxE (shrink)	17	1	582	1,018,228	1,474,085	18
XC2SxxxE	13	0	682	836,292	1,005,944	12
XC2Vxxx	20	0	893	1,624,862	2,025,201	6
XCE2Vxxx	9	0	395	792,767	1,086,039	11
XC2VPxxx	9	0	404	775,819	1,084,982	11
XCE2VPxxx	8	0	384	834,489	1,162,258	10
XC3Sxxx	10	0	445	802,610	1,017,942	12
XC3SxxxE	9	0	436	743,573	1,007,462	12

Table 2-1: **Summary of HTOL Test Results *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3SxxxA	10	0	460	877,862	1,071,159	11
XC3SxxxAN	10	0	639	776036	1,048,055	11
XC3SDxxxA	7	0	293	565,731	1,020,458	12
XC6Sxxx	6	0	295	592,956	1,230,312	10
XC4VxXxxx	10	2	514	1,029,202	2,370,606	17
XCE4VxXxxx	9	1	405	564,592	1,065,979	24
XC5VxXxxx	11	1	519	1,003,388	2,360,899	11
XCE5VxXxxx	4	0	294	339,000	877,418	13
XC6VxXxxx	8	0	328	547,588	1,023,034	12
XCE6VxXxxx	3	0	240	240,000	503,554	23
7 series FPGAs	9	0	485	931,500	1,199,840	10

Data

Table 2-2: **HTOL Test Results for 0.22/0.18 µm Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2S30	3	0	134	270,186	299,635	
XC2S50	1	0	43	86,387	93,969	
XC2S100	2	0	89	178,088	204,672	
XC2S200	4	0	180	362,160	427,094	
XC2Sxxx	10	0	446	896,821	1,025,372	11 FIT

Table 2-3: **HTOL Test Results for 0.22/0.18 µm Si Gate CMOS Device Type XCVxxx (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV300	2	0	90	180,315	202,304	
XCV400	3	0	118	216,351	238,202	
XCV600	4	0	171	348,867	401,968	
XCV800	2	0	62	124,209	135,267	
XCV1000	1	0	45	90,180	103,804	
XCVxxx	12	0	486	959,922	1,081,545	11 FIT

Table 2-4: **HTOL Test Results for 0.18 µm Si Gate CMOS Device Type XCVxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV50E	2	0	84	126,630	336,137	
XCV100E	2	0	80	115,765	115,765	
XCV200E	3	0	165	215,436	571,872	
XCV600E	4	0	118	155,046	411,568	
XCV405E	4	1(1)	209	249,914	266,058	
XCV812E	4	0	159	266,663	284,177	
XCV1000E	2	0	97	98,080	98,081	
XCV1600E	5	1(2)	195	389,099	461,936	
XCV2000E	5	1(3)	133	156,080	195,998	
XCVxxxE	31	3	1,240	1,768,713	2,741,592	20 FIT

Notes:

1. Functional failure at post 184 hours.
2. Marginal failure at post 501 hours.
3. No defect found at post 281 hours.

Table 2-5: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV100E	1	0	45	90,720	103,108	
XCV400E	2	0	90	181,800	223,121	
XCV1000E	7	0	234	359,873	580,352	
XCV2000E	5	0	168	316,231	497,900	
XCV2600E	1	1(1)	22	23,604	23,604	
XCV3200E	1	0	23	46,000	46,000	

Table 2-5: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XCVxxxE (Shrink) *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCVxxxE (shrink)	17	1	582	1,018,228	1,474,085	18 FIT

Notes:

1. No defect found at post 189 hours.

Table 2-6: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2S50E	1	0	45	90,630	100,035	
XC2S100E	5	0	230	233,162	295,897	
XC2S150E	1	0	45	91,665	110,293	
XC2S300E	4	0	272	239,395	271,134	
XC2S400E	2	0	90	181,440	228,585	
XC2SxxxE	13	0	682	836,292	1,005,944	12 FIT

Table 2-7: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2V40	3	0	135	251,190	277,242	
XC2V80	2	0	88	177,881	190,660	
XC2V250	1	0	45	68,400	79,796	
XC2V500	4	0	178	274,101	366,108	
XC2V1000	3	0	135	270,855	322,593	
XC2V1500	1	0	45	90,630	106,505	
XC2V3000	4	0	179	315,717	425,876	
XC2V4000	1	0	44	88,088	99,435	
XC2V6000	1	0	44	88,000	156,985	
XC2Vxxx	20	0	893	1,624,862	2,025,201	6 FIT

Table 2-8: **HTOL Test Results for 0.13 µm Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_J > 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC2VP2	1	0	45	92,385	106,344	
XC2VP7	1	0	45	91,305	126,841	
XC2VP20	2	0	90	140,490	216,675	
XC2VP30	3	0	134	270,334	410,189	
XC2VP40	1	0	45	90,900	90,900	
XC2VP50	1	0	45	90,045	134,033	
XC2VPxxx	9	0	404	775,819	1,084,982	11 FIT

Table 2-9: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_J > 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XCE2V1000	8	0	352	706,638	937,610	
XCE2V4000	1	0	43	86,129	148,429	
XCE2Vxxx	9	0	395	792,767	1,086,039	11 FIT

Table 2-10: **HTOL Test Results for 0.13 µm Si Gate CMOS Device Type XCE2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_J > 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XCE2VP7	2	0	134	399,152	399,152	
XCE2VP40	2	0	89	178,675	301,000	
XCE2VP50	3	0	139	234,662	410,490	
XCE2VP70	1	0	22	22,000	51,616	
XCE2VPxxx	8	0	384	834,489	1,162,258	10 FIT

Table 2-11: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq$ 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S400	4	0	175	306,035	374,236	
XC3S1000	4	0	180	361,080	463,462	
XC3S1500	2	0	90	135,495	180,244	
XC3Sxxx	10	0	445	802,610	1,017,942	12 FIT

Table 2-12: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3S250E	2	0	90	183,060	221,112	
XC3S500E	4	0	178	313,820	421,895	
XC3S700E	1	0	45	45,000	50,809	
XC3S1600E	2	0	123	201,693	313,646	
XC3SxxxE	9	0	436	743,573	1,007,462	12 FIT

Table 2-13: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3S200A	2	0	49	49,629	53,551	
XC3S700A	1	0	54	108,000	129,608	
XC3S1400A	7	0	366	738,188	885,244	
XC3SxxxxA	10	0	460	877,862	1,071,159	11 FIT

Table 2-14: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3S700AN	3	0	231	231,000	274,236	
XC3S1400AN	7	0	408	545,036	773,818	
XC3SxxxAN	10	0	639	776036	1,048,055	11 FIT

Table 2-15: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3SD1800A	2	0	90	180,135	276,987	
XC3SD3400A	5	0	203	385,596	743,471	
XC3SDxxxA	7	0	293	565,731	1,020,458	12 FIT

Table 2-16: **HTOL Test Results for 0.045 µm Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6SLX45	2	0	85	171,651	425,898	
XC6SLX45T	1	0	40	80,120	143,250	
XC6SLX75T	2	0	125	250,510	499,210	
XC6Sxxx	6	0	295	592,956	1,230,312	10 FIT

Table 2-17: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4VLX15	1	0	45	91,080	114,529	
XC4VLX40	1	0	80	160,000	233,235	
XC4VLX80	2	0	120	240,705	620,203	
XC4VLX100	1	0	45	90,585	270,781	
XC4VLX160	2	2(1)	89	174,132	721,939	
XC4VFX20	1	0	45	92,475	139,875	
XC4VFX40	1	0	45	90,225	153,416	
XC4VFX12	1	0	45	90,000	116,627	
XC4VxXxxx	10	2	514	1,029,202	2,370,606	17 FIT

Notes:

1. Failure due to substrate defect. New process improvement has been implemented.

Table 2-18: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XCE4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE4VLX80	4	1(1)	181	203,715	527,379	
XCE4VLX40	2	0	89	179,302	283,169	
XCE4VSX25	3	0	135	181,575	255,431	
XCE4VxXxx	9	1	405	564,592	1,065,979	24 FIT

Notes:

1. Failure due to substrate defect. New process improvement has been implemented

Table 2-19: **HTOL Test Results for 0.065 µm Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC5VLX155T	2	0	90	180,000	432,405	
XC5VLX110T	3	1(1)	162	286,568	483,435	
XC5VLX50T	2	0	90	180,045	623,372	
XC5VLX85T	1	0	45	91,800	182,786	
XC5VSX35T	3	0	132	264,975	638,901	
XC5VxXxxx	11	1	519	1,003,388	2,360,899	11 FIT

Notes:

1. Failure due to substrate defect. New process improvement has been implemented

Table 2-20: **HTOL Test Results for 0.065 µm Si Gate CMOS Device Type XCE5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE05VL11	3	0	249	249,000	630,879	
XCE5VL110T	1	0	45	90,000	246,539	
XCE5VxXxxx	4	0	294	339,000	877,418	13 FIT

Table 2-21: **HTOL Test Results for 0.40 µm Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6VLX130T	1	0	45	90,000	188,833	
XC6VLX240T	7	0	283	457,588	834,201	
XC6VxXxxx	8	0	328	547,588	1,023,034	12 FIT

Table 2-22: **HTOL Test Results for 0.040 µm Si Gate CMOS Device Type XCE6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE06L24T	3	0	240	240,000	503,554	
XCE6VxXxxx	3	0	240	240,000	503,554	23 FIT

Table 2-23: **HTOL Test Results for 0.028 µm Si Gate CMOS Device Type 7 Series FPGAs and Zynq-7000 SoCs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC7A100T	2	0	158	316,000	407,031	
XC7K325T	3	0	80	160,000	206,092	
XC7VH580T	2	0	48	96,000	96,000	
XC7Z020	2	0	139	246,800	317,896	
7 seriesFPGAs and Zynq-7000 SoCs	9	0	485	931,500	1,199,840	10 FIT

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C and 85% RH and VDD bias. Package preconditioning is performed on the testing samples prior to the THB test.

The failures listed in Table 2-24 are also listed by device with failure analysis results in the footnotes.

Summary

Table 2-24: **THB Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCVxxxE (Shrink)	1	0	25	25,000
XC2Vxxx	1	0	45	45,000
XC2VPxxx	4	1	180	179,000
XC2Sxxx	1	0	45	45,000
XC3Sxxx	5	0	219	219,000
XC3SxxxE	8	0	355	355,000
XC3SxxxA	1	0	45	45,000
XC3SxxxAN	3	0	75	75,000
XC4VxXxxx	5	0	221	221,000
XC5VxXxxx	6	0	270	270,900
XC6VxXxxx	5	0	225	225,000
7 series FPGAs	31	1	908	907,655

Data

Table 2-25: **THB Test Results for Si Gate CMOS Device Type XCVxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV1000E (Shrink)	1	0	25	25,000
XCVxxxE (Shrink)	1	0	25	25,000

Table 2-26: **THB Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V6000F	1	0	45	45,000
XC2Vxxx	1	0	45	45,000

Table 2-27: **THB Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2VP7	1	0	45	45,000
XC2VP30	1	0	45	45,000
XC2VP50	1	0	45	45,000
XC2VP100	1	1(1)	45	44,000
XC2VPxxx	4	1	180	179,000

Notes:

1. Failure due to substrate short caused by foreign material. New cleaning process implemented.

Table 2-28: **THB Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S30	1	0	45	45,000
XC2Sxxx	1	0	45	45,000

Table 2-29: **THB Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200	2	0	84	84,000
XC3S400	2	0	90	90,000
XC3S5000	1	0	45	45,000
XC3Sxxx	5	0	219	219,000

Table 2-30: **THB Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	3	0	132	132,000
XC3S500E	1	0	44	44,000
XC3S250E	1	0	44	44,000
XC3S1200E	2	0	90	90,000
XC3S1600E	1	0	45	45,000
XC3SxxxE	8	0	355	355,000

Table 2-31: **THB Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400A	1	0	45	45,000
XC3SxxxA	1	0	45	45,000

Table 2-32: **THB Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400AN	3	0	75	75,000
XC3SxxxAN	3	0	75	75,000

Table 2-33: **THB Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VLX15	1	0	43	43,000
XC4VLX40	1	0	45	45,000
XC4VLX60	1	0	45	45,000
XC4VLX80	1	0	45	45,000
XC4VLX100	1	0	43	43,000
XC4VxXxxx	5	0	221	221,000

Table 2-34: **THB Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX50T	2	0	90	90,000
XC5VLX85T	1	0	45	45,900
XC5VLX110T	1	0	45	45,000
XC5VLX155T	2	0	90	90,000
XC5VxXxxx	6	0	270	270,900

Table 2-35: **THB Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VLX130T	1	0	45	45,000
XC6VLX240T	3	0	135	135,000
XC6VLX365T	1	0	45	45,000
XC6VxXxxx	5	0	225	225,000

Table 2-36: **THB Test Results for Si Gate CMOS Device Type 7 Series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A100T	2	1	149	148,000
XC7A200T	2	0	89	89,000
XC7K325T	8	0	246	246,000
XC7V2000T	11	0	193	193,955
XC7VH580T	6	0	150	149,700
XC7VX1140T	2	0	81	81,000
7 series FPGAs	31	1	908	907,655

Notes:

1. 168 hour failure due to substrate metal 2 copper filament. Implemented 100% optical inspection and improved high voltage screening.

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-37: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3Sxxx	2	0	90	90,765
XC3SxxxE	1	0	45	45,315
XC3SxxxA	2	0	54	55,701
XC3SDxxxA	2	0	158	158,396
XC4VxXxxx	6	0	98	98,596
XC5VxXxxx	6	0	279	283,190
XC6VxXxxx	3	0	75	75,000
7 series FPGAs	19	0	472	472,099

Data

Table 2-38: **TH Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200	1	0	45	45,450
XC3S1500	1	0	45	45,315
XC3Sxxx	2	0	90	90,315

Table 2-39: **TH Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S500E	1	0	45	45,315
XC3SxxxE	1	0	45	45,315

Table 2-40: **TH Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400A	2	0	54	55,701

Table 2-41: **TH Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SD3400A	2	0	158	158,396

Table 2-42: **TH Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VLX80	1	0	23	23,161
XC4VLX100	5	0	75	75,435
XC4VxXxxx	6	0	98	98,596

Table 2-43: **TH Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX50T	6	0	279	283,190

Table 2-44: **TH Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VLX240T	3	0	75	75,000
XC6VxXxxx	3	0	75	75,000

Table 2-45: **TH Test Results for Si Gate CMOS Device Type 7 Series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7K325T	9	0	242	242,000
XC7K410T	3	0	81	81,000
XC7V2000T	4	0	74	74,099
XC7VH580T	3	0	75	75,000
7 series FPGAs	19	0	472	472,099

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-46: **Summary of Temperature Cycling Test Results(1)**

Device	Lot Quantity	Failures	Device on Test	Total Device Cycles
XC2Sxxx	4	0	180	180,000
XC2SxxxE	2	0	90	90,000
XCVxxxE (shrink)	2	0	50	50,000
XC2Vxxx	2	0	90	90,000
XC2VPxxx	7	0	255	255,000
XC3Sxxx	17	0	545	545,000
XC3SxxxE	25	0	943	955,500
XC3SxxxA	16	0	554	554,000
XC3SDxxxA	9	0	225	225,000
XC3SxxxAN	16	0	403	403,000
XC6Sxxx	10	0	369	369,000
XC4VxXxxx	6	0	269	269,900
XC5VxXxxx	7	0	315	315,000
XC6VxXxxx	8	1	360	359,000

Table 2-46: **Summary of Temperature Cycling Test Results(1) *(Cont'd)***

Device	Lot Quantity	Failures	Device on Test	Total Device Cycles
7 series FPGAs and Zynq-7000 SoCs	107	0	3522	3,522,953

Notes:

1. Failures listed in this table are also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-47: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2S30	B: -55°C to +125°C	1	0	45	45,000
XC2S50	B: -55°C to +125°C	2	0	90	90,000
XC2S150	B: -55°C to +125°C	1	0	45	45,000
XC2Sxxx	B: -55°C to +125°C	4	0	180	180,000

Table 2-48: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2S100E	B: –55°C to +125°C	1	0	45	45,000
XC2S200E	B: –55°C to +125°C	1	0	45	45,000
XC2SxxxE	B: –55°C to +125°C	2	0	90	90,000

Table 2-49: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCV1000E	B: -55°C to +125°C	2	0	50	50,000
XCVxxxE	B: -55°C to +125°C	2	0	50	50,000

Table 2-50: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2V80	B: -55°C to +125°C	1	0	45	45,900
XC2V6000	B: -55°C to +125°C	1	0	45	45,000
XC2Vxxx	B: -55°C to +125°C	2	0	90	90,000

Table 2-51: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2VP7	B: -55°C to +125°C	1	0	45	45,000
XC2VP30	B: -55°C to +125°C	1	0	45	45,000
XC2VP40	B: -55°C to +125°C	3	0	75	75,000
XC2VP50	B: -55°C to +125°C	1	0	45	45,000
XC2VP100	B: -55°C to +125°C	1	0	45	45,000
XC2VPxxx	B: -55°C to +125°C	7	0	255	255,000

Table 2-52: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200	B: –55°C to +125°C	2	0	90	90,000
XC3S400	B: –55°C to +125°C	2	0	90	90,000
XC3S1000	B: –55°C to +125°C	1	0	45	45,000
XC3S1500	B: –55°C to +125°C	5	0	125	125,000
XC3S5000	B: –55°C to +125°C	7	0	195	195,000
XC3Sxxx	B: –55°C to +125°C	17	0	545	545,000

Table 2-53: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S100E	B: -55°C to +125°C	3	0	134	134,000
XC3S250E	B: -55°C to +125°C	1	0	45	45,000
XC3S500E	B: -55°C to +125°C	4	0	180	180,000
XC3S1200E	B: -55°C to +125°C	5	0	205	217,500
XC3S1600E	B: -55°C to +125°C	12	0	379	379,000
XC3SxxxE	B: -55°C to +125°C	25	0	943	955,500

Table 2-54: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S50A	B: -55°C to +125°C	1	0	45	45,000
XC3S200A	B: -55°C to +125°C	2	0	90	90,000
XC3S1400A	B: -55°C to +125°C	13	0	419	419,000
XC3SxxxA	B: -55°C to +125°C	16	0	554	554,000

Table 2-55: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3SD3400A	B: –55°C to +125°C	9	0	225	225,000
XC3SDxxxA	B: –55°C to +125°C	9	0	225	225,000

Table 2-56: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S50AN	B: –55°C to +125°C	3	0	75	75,000
XC3S400AN	B: –55°C to +125°C	4	0	100	100,000
XC3S1400AN	B: –55°C to +125°C	9	0	228	228,000
XC3SxxxAN	B: –55°C to +125°C	16	0	403	403,000

Table 2-57: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX4	B: -55°C to +125°C	1	0	45	45,000
XC6SLX16	B: -55°C to +125°C	1	0	45	45,000
XC6SLX45	B: -55°C to +125°C	1	0	45	45,000
XC6SLX150	B: -55°C to +125°C	1	0	44	44,000
XC6SLX45T	B: -55°C to +125°C	1	0	45	45,000
XC6SLX100T	B: -55°C to +125°C	4	0	100	100,000
XC6SLX150T	B: -55°C to +125°C	1	0	45	45,000
XC6Sxxx	B: -55°C to +125°C	10	0	369	369,000

Table 2-58: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4VLX15	B: -55°C to +125°C	1	0	44	44,000
XC4VLX40	B: -55°C to +125°C	1	0	45	45,900
XC4VLX60	B: -55°C to +125°C	1	0	45	45,000
XC4VLX80	B: -55°C to +125°C	1	0	45	45,000
XC4VLX100	B: -55°C to +125°C	2	0	90	90,000
XC4VxXxxx	B: -55°C to +125°C	6	0	269	269,900

Table 2-59: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC5VLX50	B: -55°C to +125°C	1	0	45	45,000
XC5VLX50T	B: -55°C to +125°C	2	0	90	90,000
XC5VLX85T	B: -55°C to +125°C	1	0	45	45,000
XC5VLX110T	B: -55°C to +125°C	1	0	45	45,000
XC5VLX155T	B: -55°C to +125°C	2	0	90	90,000
XC5VXxXxxx	B: -55°C to +125°C	7	0	315	315,000

Table 2-60: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6VLX130T	B: -55°C to +125°C	2	0	90	90,000
XC6VLX240T	B: -55°C to +125°C	3	1(1)	135	134,000
XC6VLX365T	B: -55°C to +125°C	3	0	135	135,000
XC6VxXxxx	B: -55°C to +125°C	8	1	360	359,000

Notes:

1. Substrate short caused by inter-layer copper particle. Process control improvements implemented.

Table 2-61: **Temperature Cycling Test Results for Si Gate CMOS Device Type 7 Series FPGAs and Zynq-7000 SoCs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7A100T	B: -55°C to +125°C	23	0	1099	1,099,000
XC7A200T	B: -55°C to +125°C	4	0	120	120,000
XC7K325T	B: -55°C to +125°C	7	0	260	260,000
XC7K410T	B: -55°C to +125°C	14	0	382	384,516
XC7VH580T	B: -55°C to +125°C	3	0	75	75,000
XC7VH870T	B: -55°C to +125°C	3	0	76	76,000
XC7VX485T	B: -55°C to +125°C	5	0	129	127,028
XC7VX690T	B: -55°C to +125°C	23	0	614	613,975
XC7VX980T	B: -55°C to +125°C	15	0	404	404,000
XC7VX1140T	B: -55°C to +125°C	5	0	146	146,434
XC7V2000T	B: -55°C to +125°C	4	0	172	172,000
XC7Z020	B: -55°C to +125°C	1	0	45	45,000
7 series FPGAs and Zynq-7000 SoCs	B: -55°C to +125°C	107	0	3522	3,522,953

High Accelerated Stress Test

The HAST test is conducted under the conditions of 130°C, 85% RH and V_{DD} bias or 110°C, 85% RH and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-62: **Summary of HAST Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3Sxxx	5	0	125	33,000
XC3SxxxA	8	0	299	63,816
XC3SxxxAN	3	0	75	19,800
XC6Sxxx	4	0	180	39,960
XC7xxx	4	1	283	74,448

Data

Table 2-63: **HAST Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S1500	110°C, 85% RH	5	0	125	33,000
XC3Sxxx		5	0	125	33,000

Table 2-64: **HAST Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S50A	130°C, 85% RH	1	0	45	4,320
XC3S200A	110°C, 85% RH	1	0	44	11,616
XC3S1400A	110°C, 85% RH	4	0	120	31,680
XC3S1400A	130°C, 85% RH	1	0	45	4,320
XC3SxxxA		8	0	299	63,816

Table 2-65: **HAST Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S1400AN	110°C, 85% RH	3	0	75	19,800
XC3SxxxxAN		3	0	75	19,800

Table 2-66: **HAST Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX16	110°C, 85% RH	1	0	45	11,880
XC6SLX45	110°C, 85% RH	1	0	45	11,880
XC6SLX45T	110°C, 85% RH	1	0	45	11,880
XC6SLX150T	130°C, 85% RH	1	0	45	4,320
XC6Sxxx		4	0	180	39,960

Table 2-67: **HAST Test Results for Si Gate CMOS Device Type XC7xxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7A100T	110°C, 85% RH	4	1(1)	283	74,448

Notes:

1. Lifted ball bond. Tightened process controls and improved bonding recipe.

Unbiased High Accelerated Stress Test

The HASTU test is conducted under the conditions of 130°C, 85% RH or 110°C, 85% RH. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-68: **HASTU Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2Sxxx	3	0	135	12,960
XC2SxxxE	2	0	90	8,640
XC2Vxxx	1	0	45	4,320
XC3Sxxx	5	0	165	36,000
XC3SxxxE	14	0	510	100,200
XC3SxxxA	11	0	315	78,600
XC3SxxxAN	12	0	293	83,952
XC3SDxxxA	3	0	75	19,800
XC6Sxxx	1	0	45	4,320
XC7xxx	9	0	354	93,456

Data

Table 2-69: **HASTU Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S50	2	0	90	8,640
XC2S150	1	0	45	4,320
XC2Sxxx	3	0	135	12,960

Table 2-70: **HASTU Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S100E	1	0	45	4,320
XC2S200E	1	0	45	4,320
XC2SxxxE	2	0	90	8,640

Table 2-71: **HASTU Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V80	1	0	45	4,320
XC2Vxxx	1	0	45	4,320

Table 2-72: **HASTU Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S400	1	0	45	4,11,880
XC3S1000	1	0	45	4,320
XC3S1500	3	0	75	19,800
XC3Sxxx	5	0	165	36,000

Table 2-73: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	1	0	45	11,880
XC3S250E	1	0	45	11,880
XC3S500E	3	0	135	12,960
XC3S1200E	1	0	45	11,880
XC3S1200E	2	0	70	6,720

Table 2-73: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxE *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1600E	6	0	170	44,880
XC3SxxxE	14	0	510	100,200

Table 2-74: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200A	1	0	45	4,320
XC3S1400A	10	0	270	74,280
XC3SxxxA	11	0	315	78,600

Table 2-75: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S50AN	3	0	75	19,800
XC3S400AN	5	0	134	21,264
XC3S1400AN	3	0	75	26,400
XC3SxxxAN	11	0	284	67,464

Table 2-76: **HASTU Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SD3400A	3	0	75	19,800
XC3SDxxxA	3	0	75	19,800

Table 2-77: **HASTU Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX4	2	0	90	8,640
XC6SLX9	1	0	45	4,320
XC6SLX16	1	0	45	4,320
XC6Sxxx	4	0	180	17,280

Table 2-78: **HASTU Test Results for Si Gate CMOS Device Type XC7xxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A100T	9	0	354	93,456

High Temperature Storage Life

The High-Temperature Storage Life test is conducted under the conditions of 150°C and with the device unbiased.

Summary

Table 2-79: **Summary of High-Temperature Storage Life Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCVxxxE (shrink)	1	0	25	25,500
XC2Sxxx	3	0	135	135,000
XC2SxxxE	2	0	90	90,000
XC2Vxxx	1	0	45	45,000
XC3Sxxx	11	0	392	392,000
XC3SxxxE	19	0	735	785,135
XC3SxxxA	16	3	540	565,580
XC3SDxxxA	3	0	75	75,000
XC3SxxxAN	16	0	400	400,000
XC6Sxxx	4	0	180	181,080
XC6VxXxxx	1	0	40	40,320
7 series FPGAs	37	1	1,100	1,123,186

Data

Table 2-80: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV1000E	1	0	25	25,500
XCVxxxE (shrink)	1	0	25	25,500

Table 2-81: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S30	1	0	45	45,000
XC2S50	1	0	45	45,000
XC2S150	1	0	45	45,000
XC2Sxxx	3	0	135	135,000

Table 2-82: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S100E	1	0	45	45,000
XC2S200E	1	0	45	45,000
XC2SxxxE	2	0	90	90,000

Table 2-83: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V80	1	0	45	45,000
XC2Vxxxx	1	0	45	45,000

Table 2-84: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200	2	0	90	90,000
XC3S400	2	0	88	88,000
XC3S1000	1	0	45	45,000
XC3S1500	5	0	125	125,000
XC3S5000	1	0	44	44,000
XC3Sxxx	11	0	392	392,000

Table 2-85: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	2	0	90	90,135
XC3S500E	4	0	180	180,000
XC3S1200E	3	0	115	115,000
XC3S1600E	7	0	215	265,000
XC3SxxxE	19	0	735	785,135

Table 2-86: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S50A	1	0	45	45,000
XC3S200A	2	0	90	90,000
XC3S1400A	13	3(1)	405	430,580

Table 2-86: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxA *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SxxxA	16	3	540	565,580

Notes:
1. Lifted bond balls due to organic residue on pads. Tightened incoming wafer inspection.

Table 2-87: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SD3400A	3	0	75	75,000
XC3SDxxxA	3	0	75	75,000

Table 2-88: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S50AN	3	0	75	75,000
XC3S400AN	4	0	100	100,000
XC3S1400AN	9	0	225	225,000
XC3SxxxAN	16	0	400	400,000

Table 2-89: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX4	1	0	45	45,000
XC6SLX16	1	0	45	46,080
XC6SLX45T	1	0	45	45,000
XC6SLX150T	1	0	45	45,000
XC6Sxxx	4	0	180	181,080

Table 2-90: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VLX130T	1	0	40	40,320
XC6VxXxxx	1	0	40	40,320

Table 2-91: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type 7 Series FPGAs and Zynq-7000 SoCs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A100T	8	0	243	244,152
XC7K325T	7	0	194	194,000
XC7K410T	3	0	81	81,000
XC7V2000T	5	0	168	168,174
XC7VH580T	6	0	150	150,000
XC7VH870T	3	1(1)	73	71,760
XC7VX1140T	2	0	80	80,000
XC7VX485T	1	0	33	49,500
XC7Z020	2	0	78	84,600
7 series FPGAs and Zynq-7000 SoCs	37	1	1,100	1,123,186

Notes:

1. One unit failed for DCIO at post reflow due to defect at UBM plating. Corrective action is in place.

Flash PROM Products

HTOL Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

Table 2-92: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC17Vxxx/XC17SxxxA	11	0	499	968,168	1,061,222	23
XC18Vxxx	16	0	715	760,225	1,004,700	25
XCFxxxS/P	12	0	482	1,067,500	1,105,652	22

Data

Table 2-93: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC17V04	5	0	223	363,015	377,803	
XC17V08	2	0	97	198,678	208,026	
XC17V16	2	0	89	183,112	190,759	
XC17S50A	1	0	45	90,000	90,000	
XC17S200A	1	0	44	88,264	88,264	
XC17Vxx/ XC17SxxxA	11	0	499	968,168	1,061,222	23 FIT

Table 2-94: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type 18Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC18V02	6	0	265	265,000	303,152	
XC18V04	9	0	405	405,000	609,828	
XC18V512	1	0	45	90,225	91,720	
XC18Vxxx	16	0	715	760,225	1,004,700	25 FIT

Table 2-95: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCF08P	2	0	90	90,000	90,000	
XCF16P	4	0	122	730,000	730,000	
XCF32P	5	0	225	225,000	263,152	
XCF128X	1	0	45	22,500	22,500	
XCFxxxS/P	12	0	482	1,067,500	1,105,652	22 FIT

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-96: **Summary of THB Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S	6	0	209	209,000
XCFxxxS/P	8	0	360	600,480

Data

Table 2-97: **THB Test Results of Si Gate CMOS Device Type XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S50A	1	0	44	44,000
XC17S200A	5	0	165	165,000
XC17SxxxA	6	0	209	209,000

Table 2-98: **THB Test Results of Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF16P	1	0	45	75,060
XCF32P	7	0	315	525,420
XCFxxxS/P	8	0	360	600,480

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-99: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17Vxxx/XC17SxxxA	1	0	44	44,812

Data

Table 2-100: **TH Test Results of Si Gate CMOS Device Type XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S100A	1	0	44	44,812
XC17SxxxA	1	0	44	44,812

Temperature Cycling Tests

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in an air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-101: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC17SxxxA	7	0	225	255,000
XCFxxxS/P	6	0	270	441,180

Data

Table 2-102: **Temperature Cycling Test Results for Si Gate CMOS Device**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC17S50A	B: –55°C to +125°C	1	0	45	45,000
XC17S100A	B: –55°C to +125°C	1	0	45	45,000
XC17S200A	B: –55°C to +125°C	5	0	165	165,000
XC17SxxA	B: –55°C to +125°C	7	0	225	255,000

Table 2-103: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCF32P	C: –65°C to +150°C	6	0	270	441,180
XCFxxxS/P	C: –65°C to +150°C	6	0	270	441,180

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% RH (unbiased), and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-104: **Summary of Autoclave Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17SxxxA	1	0	45	4,320
XCFxxxS/P	6	0	270	25,920

Data

Table 2-105: **Autoclave Test Results for Si Gate CMOS Device Type XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S15A	1	0	45	4,320
XC17SxxxA	1	0	45	4,320

Table 2-106: **Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF32P	6	0	270	25,920
XCFxxxS/P	6	0	270	25,920

Unbiased High Accelerated Stress Test

The HASTU test is conducted under the conditions of 130°C, 85% RH or 110°C, and 85% RH. Package preconditioning is performed on the testing samples prior to the HASTU test.

Summary

Table 2-107: **Summary of HASTU Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17SxxxA	2	0	90	16,200

Data

Table 2-108: **HASTU Test Results for Si Gate CMOS Device Type XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S100A	1	0	45	4,320
XC17S50A	1	0	45	11,880
XC17SxxxA	2	0	90	16,200

Program/Erase Endurance Test

The Program/Erase Endurance test is conducted under nominal voltage and room temperature.

Qualification Data

Table 2-109: **Program/Erase Endurance Test Results of Si Gate CMOS Device Type XC18Vxxx/XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC18V04	1	0	32	640,000
XCF08P	1	0	16	320,000
XCF16P	2	0	93	1,860,000
XCF32P	2	0	93	1,860,000

Data Retention Bake Test

The data retention bake test is conducted at 150°C ambient temperature. The devices are programmed prior to the bake test.

Summary

Table 2-110: **Summary of Data Retention Bake Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17Vxxx/XC17SxxxA	8	0	300	300,000
XCFxxxS/P	6	0	270	450,360

Data

Table 2-111: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC17SxxxA/XC17Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17V16	1	0	45	45,000
XC17S50A	1	0	45	45,000
XC17S100A	1	0	45	45,000
XC17S200A	5	0	165	165,000
XC17SxxxA/XC17Vxxx	8	0	300	300,000

Table 2-112: **Data Retention Bake Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF32P	6	0	270	450,360
XCFxxxS/P	6	0	270	450,360

CPLD Products

HTOL Tests

The HTOL test is conducted under the conditions of T_J > 125°C temperature, maximum V_{DD}, and either dynamic or static operation. The FIT calculations in Table 2-113 through Table 2-116 are based on the assumption of 0.7 eV activation energy and 60% confidence level.

Summary

Table 2-113: **Summary of HTOL Test Results(1)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC95xxxXL	20	0	1100	1,623,331	2,249,421	5
XCRxxxXL	12	0	535	1,074,715	1,076,451	11
XC2Cxxx/A	12	0	538	1,059,372	1,062,604	11

Notes:

1. Failures listed in this table are also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-114: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC95128XL	1	0	45	90,630	231,398	
XC95144XL	6	0	298	480,880	656,058	
XC95288XL	8	0	472	611,310	821,688	
XC9572XL	5	0	285	440,691	540,276	
XC95xxxXL	20	0	1100	1,623,331	2,249,421	5 FIT

Table 2-115: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Devices	Lot Quantity	Failures	Device on Test	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCR3128XL	3	0	135	270,855	271,487	
XCR3256XL	4	0	176	351,868	253,614	
XCR3384XL	4	0	176	355,416	355,774	
XCR3512XL	1	0	48	96,576	96,576	
XCRxxxXL	12	0	535	1,074,715	1,076,451	11 FIT

Table 2-116: **HTOL Test Results of 0.18 µm Si Gate CMOS Device Type XC2Cxxx/A**

Devices	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2C128	2	0	90	181,350	181,690	
XC2C256	5	0	223	426,942	428,364	
XC2C384	4	0	180	360,990	361,868	
XC2C512	1	0	45	90,090	90,682	
XC2Cxxx/A	12	0	538	1,059,372	1,062,604	11 FIT

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Data

Table 2-117: **THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C64A	2	0	79	79,000
XC2C128	1	0	45	45,000
XC2C256	4	0	244	244,000
XC2C384	2	0	97	97,000
XC2Cxxx/A	9	0	465	465.000

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-118: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95xxxXL	3	0	135	135,990
XCRxxxXL	2	0	69	128,985
XC2Cxxx/A	3	0	120	120,915

Data

Table 2-119: **TH Test Results of Si Gate CMOS Device Type XC95xxxXL (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	1	0	45	45,315
XC95144XL	2	0	90	90,675
XC95xxxXL	3	0	135	135,990

Table 2-120: **TH Test Results of 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3256XL	2	0	69	69,690
XCRxxxXL	2	0	69	69,690

Table 2-121: **TH Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C64A	2	0	90	135,990
XC2C256	1	0	30	30,240
XC2Cxxx/A	3	0	120	120,915

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-122: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxxXL	3	0	135	135,000
XCRxxxXL	5	0	165	165,000
XC2Cxxx/A	11	0	591	591,000

Data

Table 2-123: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9572XL	B: -55°C to +125°C	1	0	45	45,000
XC95144XL	B: -55°C to +125°C	1	0	45	45,000
XC95288XL	B: -55°C to +125°C	1	0	45	45,000
XC95xxxXL	B: -55°C to +125°C	3	0	135	135,000

Table 2-124: **Temperature Cycling Test Results of Si Gate CMOS Device Type XCRxxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCR3064XL	B: –55°C to +125°C	1	0	45	45,000
XCR3128XL	B: –55°C to +125°C	1	0	45	45,000
XCR3384XL	B: –55°C to +125°C	3	0	75	75,000
XCRxxxXL	B: –55°C to +125°C	5	0	165	165,000

Table 2-125: **Temperature Cycling Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2C64A	B: -55°C to +125°C	3	0	135	135,000
XC2C128	B: -55°C to +125°C	1	0	45	45,000
XC2C256	B: -55°C to +125°C	6	0	334	334,000
XC2C384	B: -55°C to +125°C	1	0	77	77,000
XC2Cxxx/A	B: -55°C to +125°C	11	0	591	591,000

Unbiased High Accelerated Stress Test

The HASTU test is conducted under the conditions of 130°C and 85% RH or 110°C and 85% RH. Package preconditioning is performed on the testing samples prior to the HASTU test.

Summary

Table 2-126: **HASTU Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxxXL	3	0	135	12,960
XCRxxxXL	2	0	90	8,640
XC2Cxxx/A	7	0	411	47,016

Data

Table 2-127: **HASTU Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9536XL	1	0	45	4,320
XC9572XL	1	0	45	4,320

Table 2-127: **HASTU Test Results for Si Gate CMOS Device Type XC95xxxXL *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95144XL	1	0	45	4,320
XC95xxxXL	3	0	135	12,960

Table 2-128: **HASTU Test Results for Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCR3064XL	1	0	45	4,320
XCR3128XL	1	0	45	4,320
XCRxxxXL	2	0	90	8,640

Table 2-129: **HASTU Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2C256	1	0	45	11,880
XC2C256	4	0	244	23,424
XC2C384	1	0	77	7,392
XC2C64A	1	0	45	4,320
XC2Cxxx/A	7	0	411	47,016

Program/Erase Endurance Test

The Program/Erase Endurance test is conducted under nominal voltage and predefined temperature.

Qualification Data

Table 2-130: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL; Test Condition at –40°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XL	1	0	21	420,000

Table 2-131: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL; Test Condition at 70°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XL	1	0	32	320,000

Table 2-132: **Erase Endurance Test Results of Si Gate CMOS Device Type XCRxxx/XL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3128	1	0	10	10,000
XCR3032XL	2	0	57	684,000

Data Retention Bake Test

The Data Retention Bake Test is conducted at 150°C. The devices are programmed prior to the bake test.

Summary

Table 2-133: **Summary of Data Retention Bake Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxxXL	5	0	224	224,000
XCRxxxXL	4	0	180	180,000
XC2Cxxx/A	14	0	590	590,000

Data

Table 2-134: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9536XL	1	0	45	45,000
XC9572XL	1	0	44	44,000
XC95144XL	2	0	90	90,000
XC95288XL	1	0	45	45,000
XC95xxxXL	5	0	224	224,000

Table 2-135: **Data Retention Bake Test Results of Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3064XL	1	0	45	45,000
XCR3128XL	1	0	45	45,000
XCR3256XL	2	0	90	90,000
XCRxxxXL	4	0	180	180,000

Table 2-136: **Data Retention Bake Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C128	3	0	135	135,000
XC2C256	6	0	230	230,000
XC2C384	1	0	45	45,000
XC2C512	1	0	45	45,000
XC2C64A	3	0	135	135,000
XC2Cxxx/A	14	0	590	590,000

Results by Package Type

Reliability Data for Non-Hermetic Packages

BG352, BG432, BG560

Table 3-1: **Test Results for Device Types XCV1000E, XCV1600E, XCV300**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	4	0	120	120,000
Temperature humidity 85°C, 85% RH with bias	1	0	30	30,000
HTS	1	0	45	45,000

CP56

Table 3-2: **Test Results for Device Types XCR3064XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

CP132

Table 3-3: **Test Results for Device Types XC2C256**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	43	43,000

Table 3-3: **Test Results for Device Types XC2C256 *(Cont'd)***

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HASTU	1	0	45	11,880
HTS	1	0	45	45,000

CS144

Table 3-4: **Test Results for Device Types XCV50, XC2V80**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling 85°C, 85% RH with bias	1	0	45	45,900
HTS	1	0	45	45,000

CS324

Table 3-5: **Test Results for Device Types XC6SLX45, XC6SLX45T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
HAST	1	0	45	11,880

FB676

Table 3-6: **Test Results for Device Types XC7K325T, XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	6	0	191	191,000

FF484, FF784

Table 3-7: **Test Results for Device Types XC6SLX45T, XC6VLX130T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	90	90,000
HAST	1	0	45	11,880

FF665, FF668, FF672, FF676

Table 3-8: **Test Results for Device Types XC4VLX25, XC4VLX60F, XC4VFX20, XC4VLX40, and XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000

FF896, FF900, FF901

Table 3-9: **Test Results for Device Types XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature humidity 85°C, 85% RH with bias	3	0	81	81,000
Temperature humidity 85°C, 85% RH with bias	3	0	81	81,000
HTS	4	0	113	113,000

FF1136, FF1148, FF1152, FF1153, FF1154, FF1155, FF1156, FF1157, FF1158

Table 3-10: **Test Results for Device Types XC2V6000F, XC2VP40, XC2VP40F, XC2VP50F, XC4VLX80F, XC5VLX85T, XC6VLX240T, XC7VX485T, and XC7VX690T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	19	1(1)	635	635,188
Temperature humidity 85°C, 85% RH with bias	7	0	315	315,000

Notes:

1. Substrate short caused by inter-layer copper particle. Process control improvements implemented.

FF1696, FF1704, FF1738, FF1759, FF1760, FF1761

Table 3-11: **Test Results for Device Types XC6VLX365T, XC7V690T, and XC7V485T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	97	95,245

FF1923, FF1924, FF1925, FF1926, FF1927, FF1928, FF1929, FF1930

Table 3-12: **Test Results for Device Types XC6VHX565T, XC7VX485T, XC7VX690T, and XC7VX980T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	9	0	241	240,570
HTS	1	0	33	49.500

FG256

Table 3-13: **Test Results of Device Types XC2V80**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HASTU	1	0	45	4,320

FG320

Table 3-14: **Test Results of Device Types XC3S1600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	4	0	120	120,000
HASTU	4	0	120	31,680
HTS	4	0	120	170,000

FG324, FG456, FG484

Table 3-15: **Test Results of Device Types XC2V250, XC3S1000, XC3S1500, XC6SLX45T, XC6SLX150T, XC2S300E, and XCR3512XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	4	0	120	120,000
HTS	1	0	45	45,000

FG676

Table 3-16: **Test Results for Device Types XC2VP20, XC3S1400A, XC3S1500, XC3SD1800A, XC6SLX100T, XC3SD3400A, and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	14	0	407	407,000
HAST	6	0	150	39,600
HASTU	9	0	225	59,400
HTS	12	0	300	350,000

FS48

Table 3-17: **Test Results for Device Types XCF08P, XCF16P, and XCF32P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	1	0	45	75,060
Temperature humidity 85°C, 85% RH with bias	1	0	45	75,060
PP	1	0	45	4,320
HTS	1	0	45	75,060

FT256

Table 3-18: **Test Results for Device Types XCR3512XL, XC2S150E, XC2S300E, XC2S400E, XC2C512, XC3S1000, XC3S200A, XC3S1200E, XC3S400AN, XC3S200, XC3S50A, and XC3S200A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	6	0	190	190,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	90,000
HASTU	4	0	120	31,680
HTS	6	0	190	190,000

PC44

Table 3-19: **Test Results for Device Types XC18V04, XC9572XL, XCR3064XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	1	0	45	45,000

PD8

Table 3-20: **Test Results for Device Types XC17S200A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling -55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000
HTS	1	0	45	45,000

PQ160, PQ208

Table 3-21: **Test Results for Device Type XC95288XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling -55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000
HTS	1	0	45	45,000

SF363

Table 3-22: **Test Results for Device Types XC4VLX15F**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling -55°C to +125°C	1	0	44	44,000
Temperature humidity 85°C, 85% RH with bias	1	0	43	43,000

SO20

Table 3-23: **Test Results for Device Types XC17S100A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

TQ100 TQ144

Table 3-24: **Test Results for Device Types XC2C256, XC2C384, XC2S50E, XC2S100/E, XC3S50A, XC3S200, XC3S400, and XC95288XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	5	0	165	165,000
HASTU	4	0	120	24,210
HTS	6	0	210	210,000

VO20 and VO48

Table 3-25: **Test Results for Device Types XCF08P, XCF32P, XC18V01, XC18V02, and XC18V04**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	2	0	90	144,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	150,120
PP	2	0	90	8,640
HTS	1	0	45	75,060

VQ44, VQ100

Table 3-26: **Test Results for Device Types XC18V02, XC18V04, XC2C128, XC9572XL, XC3S200, and XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
HTS	1	0	45	45,000
HASTU	1	0	45	4,320

Reliability Data for Hermetic Packages

Reliability Data for PGA Packages

Table 3-27: **Tests of Package Types PG84, PG120, PG156, PG191, PG223, PG299, and PG475**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	15	0	
B3	Solderability	15	0	
B5	Bond strength	24	0	
D1	Physical dimension	30	0	
D2	Lead integrity	30	0	
	Seal			
D3	Thermal shock	30	0	450
	Temperature cycle			
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical shock	30	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			

Table 3-27: **Tests of Package Types PG84, PG120, PG156, PG191, PG223, PG299, and PG475 *(Cont'd)***

Code	Test	Sample Quantity	Failures	Total Device Cycles
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	30	0	
D7	Adhesion of lead finish	30	0	
D8	Lid torque	15	0	

Reliability Data for CB Packages

Table 3-28: **Tests of Package Types CB196 and CB228**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	48	0	
B3	Solderability	27	0	
B5	Bond strength	36	0	
D1	Physical dimension	60	0	
D2	Lead integrity	60	0	
	Seal			
D3	Thermal shock	60	0	
	Temperature cycle			
	Seal			
	Visual examination			
	End-Point electrical			
	Parametrics			
D4	Mechanical shock	60	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			
D5	Salt atmosphere	60	0	
	Seal			
	Visual examination			

Table 3-28: **Tests of Package Types CB196 and CB228 *(Cont'd)***

Code	Test	Sample Quantity	Failures	Total Device Cycles
D6	Internal water-vapor content	60	0	
D7	Adhesion of lead finish	60	0	
D8-LID	Lid Torque	30	0	
HTOL	Life Test	45	0	

Table 3-29: **Tests of Package Type DD8**

Code	Test	Sample Quantity	Failures	Total Device Cycles
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	30	0	
D7	Adhesion of lead finish	30	0	
D8	Lead torque	15	0	

Reliability Data for CF1144 Package

Table 3-30: **Tests of Package Type CF1144**

Code	Test	Sample Quantity	Failures	Total Device Cycles
D3	Thermal shock	15	0	225
	Parametrics			
D4	Mechanical shock	15	0	
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HAST (130°C, 85% RH)	18	0	1,728
TCB	Temperature cycling-55 to +125°C	14	0	29,260

Reliability Data for CG717 Package

Table 3-31: **Tests of Package Type CG717**

Code	Test	Sample Quantity	Failures	Total Device Cycles
	Thermal shock	15	0	225
	Mechanical shock	15	0	
	Vibration	15	0	225
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HTOL	44	0	44,000

Reliability Data for Pb-Free Packages

BGG352, BGG432, BGG560

Table 3-32: **Test Results for Device Types XCV300E (Shrink), XCV600E (Shrink), XCV1000E (Shrink)**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	50	50,000
Temperature humidity 85°C, 85% RH with bias	1	0	25	25,000
HTS	1	0	25	25,000

CLG400, CLG484

Table 3-33: **Test Results for Device Types XC7Z020**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	90	90,000
HAST	1	1(1)	44	11,616
HTS	2	0	78	84,600

Notes:

1. Lifted ball bond. Tightened process controls and improved bonding recipe.

CPG132

Table 3-34: **Test Results for Device Types XC2C256, XC2C128, XC3S250E, XC3S100E, and XC3S500E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	180	180,000
Temperature humidity 85°C, 85% RH with bias	3	0	134	134,000
HASTU	2	0	90	8,640
HTS	5	0	225	225,000

CPG196

Table 3-35: **Test Results for Device Type XC6SLX4, XC6SLX16**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

CSG144

Table 3-36: **Test Results of Device Types XC95144XL, XCR3128XL, XCS20XL, and XCV200E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

CSG324

Table 3-37: **Test Results of Device Types XC6SLX16, XC6SLX25T, XC6SLX45T, and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	7	0	365	365,000
HAST	1	0	45	11,880
HTS	1	0	45	46,080

CSG484

Table 3-38: **Test Results of Device Type XC3SD3400A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	75	75,000

FBG484

Table 3-39: **Test Results of Device Types XC7A200T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH no bias	1	0	44	44,000

FBG676

Table 3-40: **Test Results of Device Types XC7K325T, XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	10	0	262	264,080
Temperature humidity 85°C, 85% RH no bias	3	0	81	81,000
HTS	3	0	81	81,000

FBG900

Table 3-41: **Test Results of Device Types XC7K325T, XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	42	42,000

FFG323, FFG324, FFG363

Table 3-42: **Test Results of Device Types XC5VLX50**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000

FFG484, FFG784

Table 3-43: **Test Results of Device Types XC6VLX130T and XC6VLX240T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	2	0	50	50,000

FFG665, FFG668, FFG672, FFG676

Table 3-44: **Test Results of Device Types XC2VP7F, XC4VFX20F, XC4VLX60, XC5VLX110, XC7K325T, and XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000

FFG896, FFG900, FFG901

Table 3-45: **Test Results of Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	7	0	204	204,000
Temperature humidity 85°C, 85% RH no bias	6	0	162	162,000
HTS	7	0	194	194,000

FFG1136, FFG1148, FFG1152, FFG1153, FFG1154, FFG1155, FFG1156, FFG1157, FFG1158

Table 3-46: **Test Results of Device Types XC2V4000, XC2VP20F, XC2VP50, XC4VLX100, XC4VLX100F, XC4VLX40F, XC4VLX80, XC5VLX110T, XC5VLX115T, XC5VLX50T, XC5VLX85T, XC6VLX195T, XC6VLX240T, XC6VLX365T, XC6VSX475T, XC7V485T, XC7VX690T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	29	0	960	960,900
Temperature humidity 85°C, 85% RH with bias	10	0	448	448,900

FFG1513, FFG1517

Table 3-47: **Test Results of Device Types XC4VLX100F**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000

FFG1696, FFG1704, FFG1738, FFG1759, FFG1760, FFG1761

Table 3-48: **Test Results of Device Types XC2VP100F, XC5VLX330T, XC6VSX475T, XC7V485T, XC7V690T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	97	95,245
Temperature humidity 85°C, 85% RH with bias	1	1(1)	44	44,000

Notes:

1. Failure due to substrate short caused by foreign material. New cleaning process implemented.

FFG1923, FFG1924, FFG1925, FFG1926, FFG1927, FFG1928, FFG1929, FFG1930

Table 3-49: **Test Results of Device Types XC6VHX565T, XC6VHX255T and XC6VHX380T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	18	0	483	482,570
HTS	1	0	33	49,500

FGG256

Table 3-50: **Test Results of Device Types XC2S50, XC2V500**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000
Temperature cycling –55 to +125°C	3	0	135	135,000
HASTU	2	0	90	8,640
HTS	1	0	45	45,000

FGG320

Table 3-51: **Test Results of Device Types XC3S200A, XC3S400A, XC3S1200E and XC3S1600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	120	120,000
HASTU	4	0	120	31,680
HTS	4	0	120	170,000

FGG324, FGG456, and FGG484

Table 3-52: **Test Results of Device Types XC2C384, XC3S400, XC3S1000, XC3S1600E, XC3S700AN, XC3S1400A, XC6SLX45T, XC6SLX150T and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	18	0	863	863,000
Temperature humidity 85°C, 85% RH with bias	4	1(1)	238	238,000
HASTU	5	0	275	68,040
HAST	5	0	328	79,032
HTS	8	0	343	344,152

Notes:

1. 168 hour failure due to substrate metal 2 copper filament. Implemented 100% optical inspection and improved high voltage screening.

FGG400

Table 3-53: **Test Results of Device Type XC3S1200E and XC3S1600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	4,320
HASTU	1	0	45	45,000
HTS	1	0	45	45,000

FGG676

Table 3-54: **Test Results of Device Types XC2VP20, XC2VP40, XC3S1400A, XC3S1400AN, XC3S1500, XC3SD1800A, XC3SD3400A, XC6SLX100T, and XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	50	0	1387	1,387,000
Temperature humidity 85°C, 85% RH with bias	5	0	165	165,000
HAST	12	0	320	84,840
HASTU	28	0	732	199,848
HTS	34	3(1)	926	976,000

Notes:

1. Lifted bond balls due to organic residue on pads. Tightened incoming wafer inspection.

FGG900

Table 3-55: **Test Results of Device Type XC6SLX150T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	4	0	119	119,000

FHG1761

Table 3-56: **Test Results of Device Types XC7V2000T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	41	41,000
Temperature humidity 85°C, 85% RH with bias	6	0	118	118,819
Temperature humidity 85°C, 85% RH no bias	3	0	46	46,099
High temperature storage	2	0	56	56,320

FLG1925, FLG1926, FLG1928

Table 3-57: **Test Results of Device Types XC7VX1140T, XC7V2000T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	8	0	277	277,434
Temperature humidity 85°C, 85% RH with bias	7	0	156	156,136
Temperature humidity 85°C, 85% RH no bias	1	0	28	28,000
HTS	6	0	232	232,174

FSG48

Table 3-58: **Test Results for Device Types XCF08P, XCF16P, and XCF32P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	1	0	45	75,060
Temperature humidity 85°C, 85% RH with bias	1	0	45	75,060
PP	1	0	45	4,320
HTS	1	0	45	75,060

FTG256

Table 3-59: **Test Results for Device Types XC2S100E, XC2S150E, XC3S1200E, XC3S1400A, XC3S200, XC3S200A, XC3S200AN, XC3S400, XC3S400AN, XC3S500E, XC3S50A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	10	0	370	370,000
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000
HAST	4	0	179	32,136
HASTU	4	0	120	24,120
HTS	9	0	325	326,080

HCG1155

Table 3-60: **Test Results of Device Types XC7VH580T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	75	75,000
Temperature humidity 85°C, 85% RH with bias	6	0	150	149,700
Temperature humidity 85°C, 85% RH no bias	3	0	75	75,000
HTS	6	0	150	150,000

HCG1932

Table 3-61: **Test Results of Device Types XC7VH870T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	76	76,000
HTS	3	—(1)	76	76,000

Notes:

1. One unit failed for DCIO at post reflow due to defect at UBM plating. Corrective action is in place.

PCG44

Table 3-62: **Test Results for Device Types XC9572XL, XC18V02**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

PDG8

Table 3-63: **Test Results for Device Types XC17S200A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	4	0	120	120,000
Temperature humidity 85°C, 85% RH with bias	4	0	120	120,000
HTS	4	0	120	120,000

PQG160, PQG208, PQG240

Table 3-64: **Test Results of Device Types XCV200, XC2C512, XC2S150, XC2S200E, XC3S500E, XC4020XLA, and XCR3256XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	5	0	225	225,000
Temperature humidity 85°C, 85% RH with bias	2	0	89	89,000
HASTU	3	0	135	12,960
HTS	7	0	315	315,000

QFG32, QFG48

Table 3-65: **Test Results for Device Types XC2C64A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	3	0	135	270,000
Temperature humidity 85°C, 85% RH with bias	2	0	79	79,000
HASTU	1	0	45	4,320
HTS	3	0	135	135,000

SFG363

Table 3-66: **Test Results of Device Types XC4VLX15**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	44	44,000
Temperature humidity 85°C, 85% RH with bias	1	0	43	43,000

SOG20

Table 3-67: **Test Results for Device Types XC17S50A, XC17S100A, and XC18V01**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	1	0	45	45,000
HTS	1	0	45	45,000

TQG100, TQG144

Table 3-68: **Test Results of Device Types XC2C384, XC2S100E, XC2S30, XC2S50E, XC3S200, XC3S250E, XC3250AN, XC6SLX9, XC9572XL, and XCR3384XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	11	0	407	407,000
Temperature humidity 85°C, 85% RH with bias	4	0	179	179,000

Table 3-68: **Test Results of Device Types XC2C384, XC2S100E, XC2S30, XC2S50E, XC3S200, XC3S250E, XC3250AN, XC6SLX9, XC9572XL, and XCR3384XL *(Cont'd)***

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
HASTU	8	0	332	52,032
HTS	9	0	345	345,000

VQG44, VQG64, VQG100

Table 3-69: **Test Results of Device Types XC2C128, XC2C256, XC2C64A, XC3S100E, XC3S250E, XC9572XL, XCS10, XCS20XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycle
Temperature cycling –55 to +125°C	6	0	333	333,000
Temperature humidity 85°C, 85% RH with bias	4	0	245	245,000
HASTU	4	0	244	23,424
HTS	7	0	274	274,135

Board-Level Reliability Tests, SnPb Eutectic

FG676, FG680, FG900, FG1156, BF957, FF672, FF896, FF1152, FF1704, SF363, and CF1144

Table 3-70: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FG680	40 x 40	680	1.00	0.60	0.46	SMD	20.3 x 20.3 x 0.3	0.98 thick, 3-layer
FG900	31 x 31	900	1.00	0.60	0.46	SMD	17.0 x 17.0 x 0.3	0.56 thick, 4-layer
FG1156	35 x 35	1,156	1.00	0.60	0.46	SMD	23 x 21 x 0.3	0.56 thick, 4-layer
BF957	40 x 40	957	1.27	0.75	0.61	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF672	27 x 27	672	1.00	0.60	0.53	SMD	12 x 10 x 0.7	1.152 thick, 6-layer
FF896	31 x 31	896	1.00	0.60	0.53	SMD	10 x 10 x 0.7	1.152 thick, 6-layer
FF1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	26 x 22 x 0.7	1.152 thick, 6-layer

Table 3-70: **Package Details (All Dimensions in mm) *(Cont'd)***

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
SF363	17 x 17	363	0.8	0.50	0.40	SMD	10 x 10 x 0.3	0.60 thick, 4-layer
CF1144	35 x 35	1,144	1.00	0.52	0.80	SMD	22 x 20 x 0.7	1.59 thick, 10-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, HASL finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power/GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- 0°C – 100°C, 10 minutes dwells, 5 minutes ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: Resistance of net > threshold resistance (300Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-71: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FG676	7,027	30	30	4,686	6,012
FG680	4,000	30	0	NA	NA
FG900	7,027	28	28	4,405	5,344
FG1156	5,000	32	25	2,786	4,892
BF957	4,145	35	35	1,958	3,662
FF672	5,840	30	30	3,764	4,881
FF896	7,027	12	10	5,607	6,783
FF1152	4,158	30	30	2,668	3,822
FF1704	4,150	35	35	3,003	3,389
SF363 (Lot 1)	2,370	24	21	1,642	2,048
SF363 (Lot 2)	2,288	24	24	1,555	1,999
CF1144	5,000	21	0	NA	NA

Weibull Plots

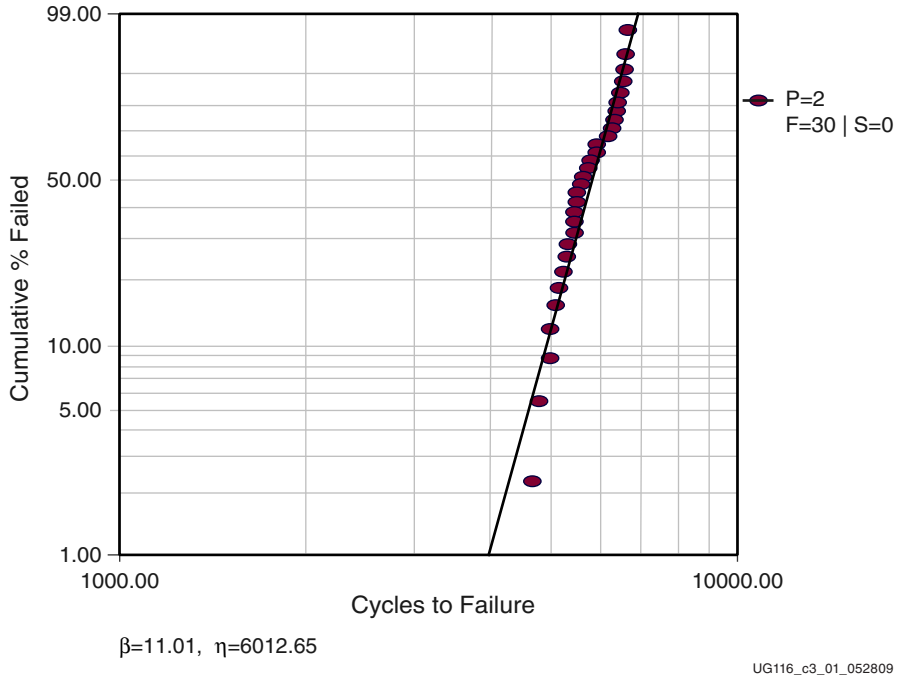

Figure 3-1: **Cycles to Failure in the Second-Level Reliability Tests for FG676**

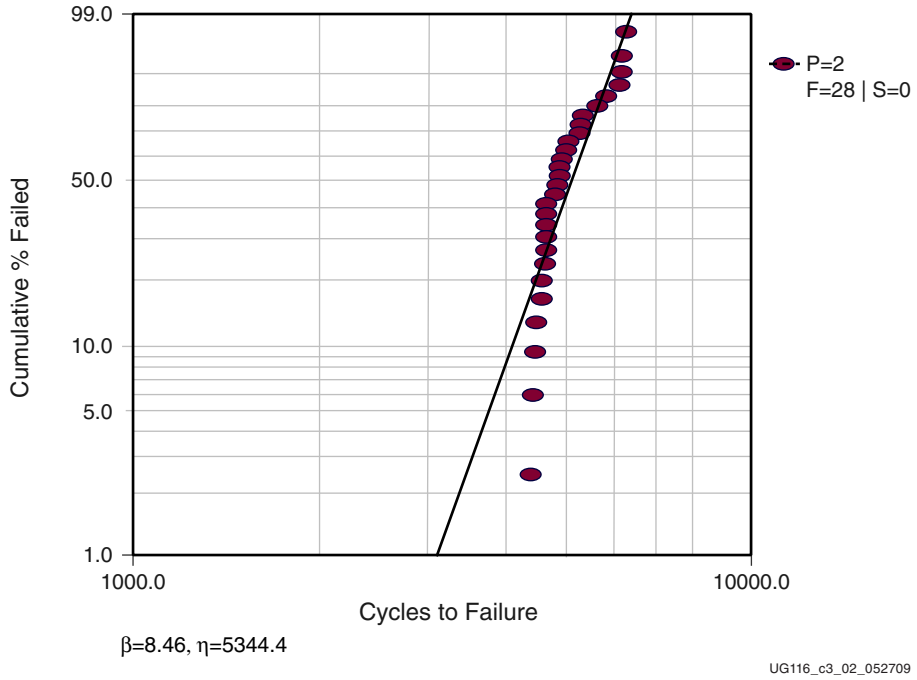

Figure 3-2: **Cycles to Failure in the Second-Level Reliability Tests for FG900**

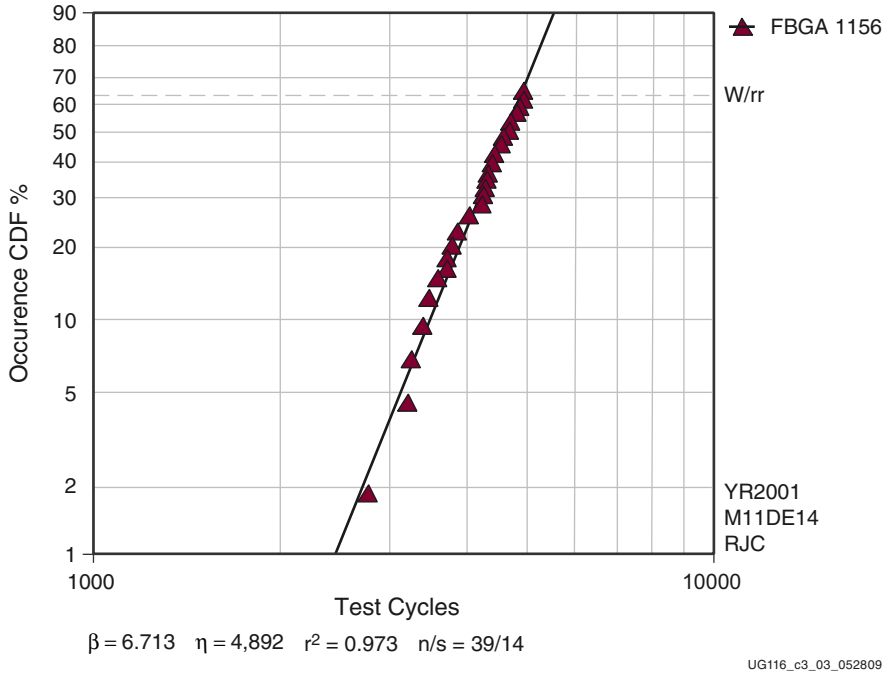

Figure 3-3: **Cycles to Failure in the Second-Level Reliability Tests for FG1156**

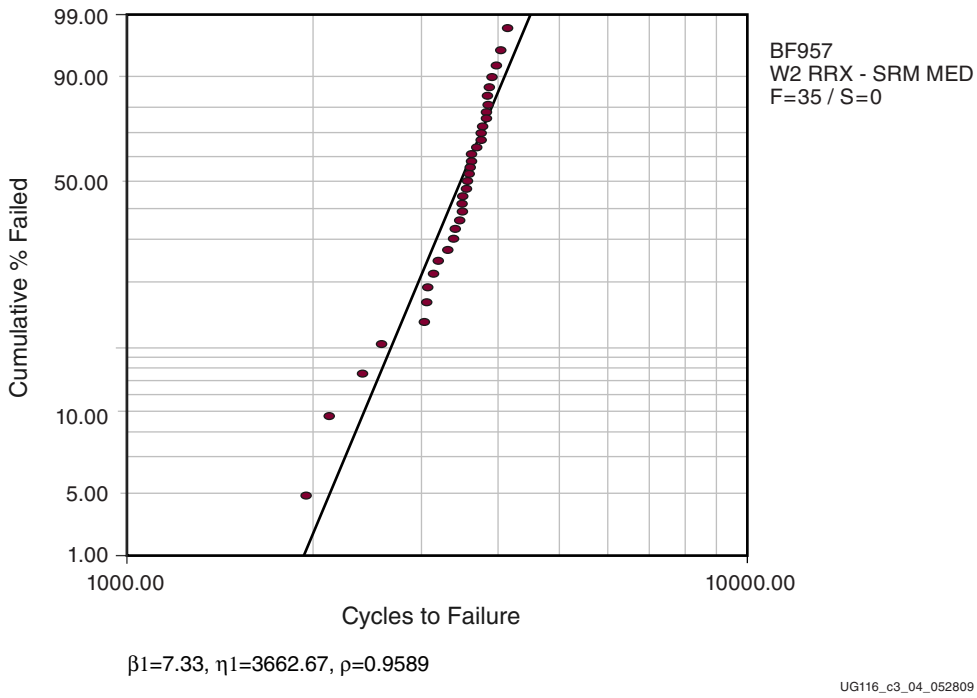

Figure 3-4: **Cycles to Failure in the Second-Level Reliability Tests for BF957**

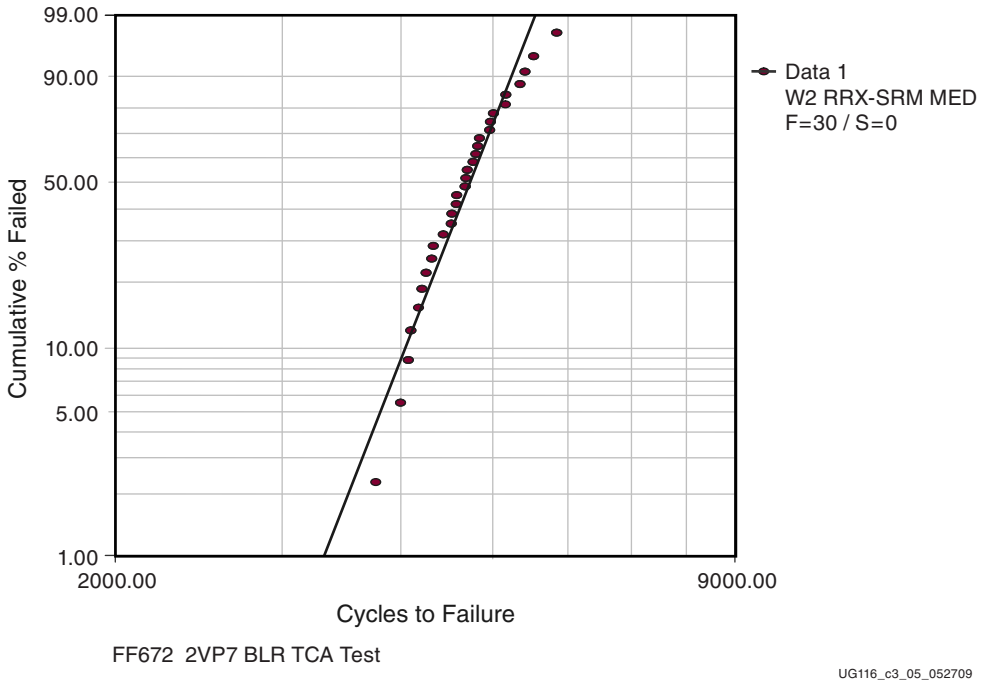

Figure 3-5: **Cycles to Failure in the Second-Level Reliability Tests for FF672**

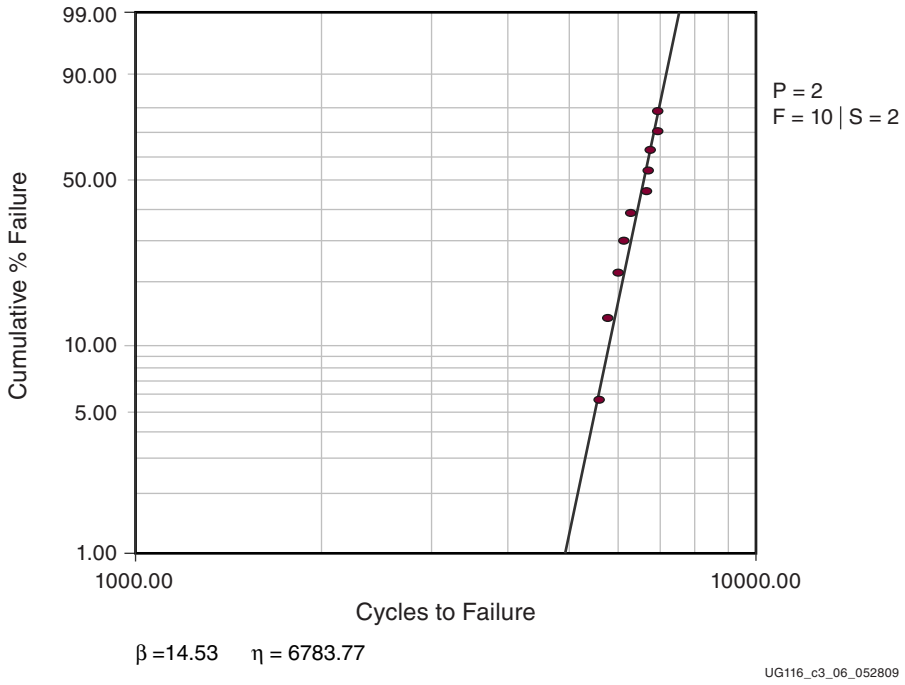

Figure 3-6: **Cycles to Failure in the Second-Level Reliability Tests for FF896**

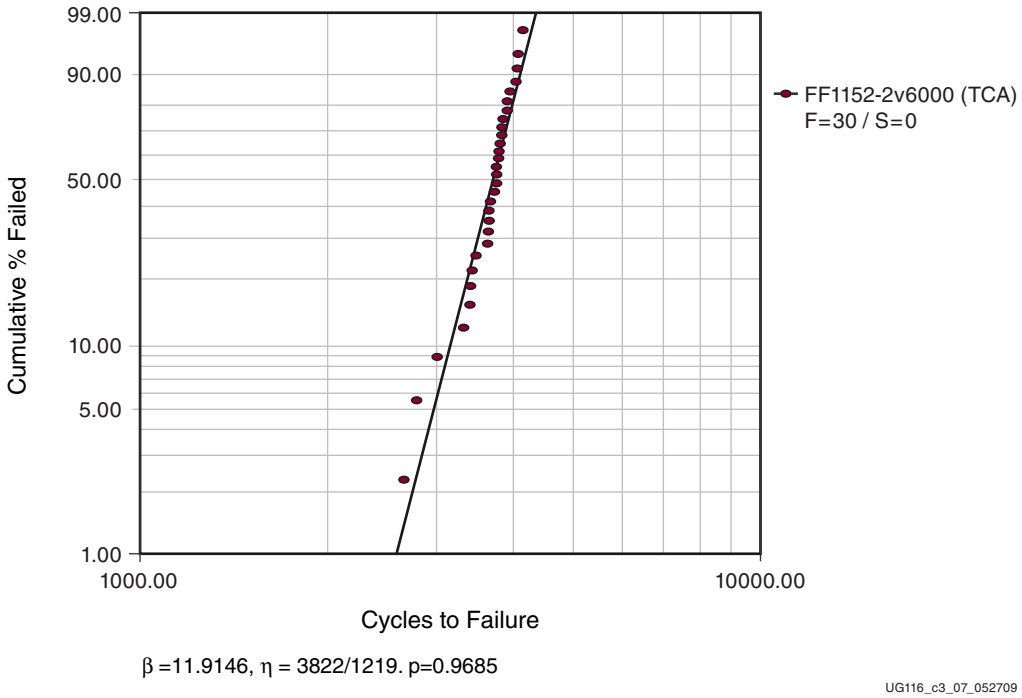

Figure 3-7: **Cycles to Failure in the Second-Level Reliability Tests for FF1152**

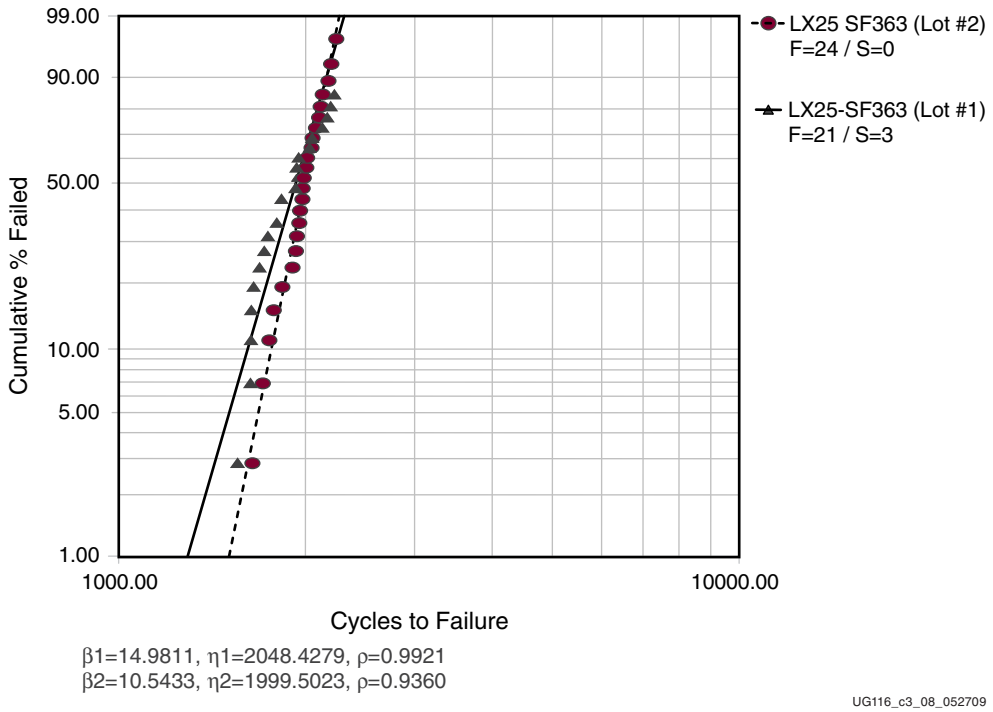

Figure 3-8: **Cycles to Failure in the Second-Level Reliability Tests for SF363**

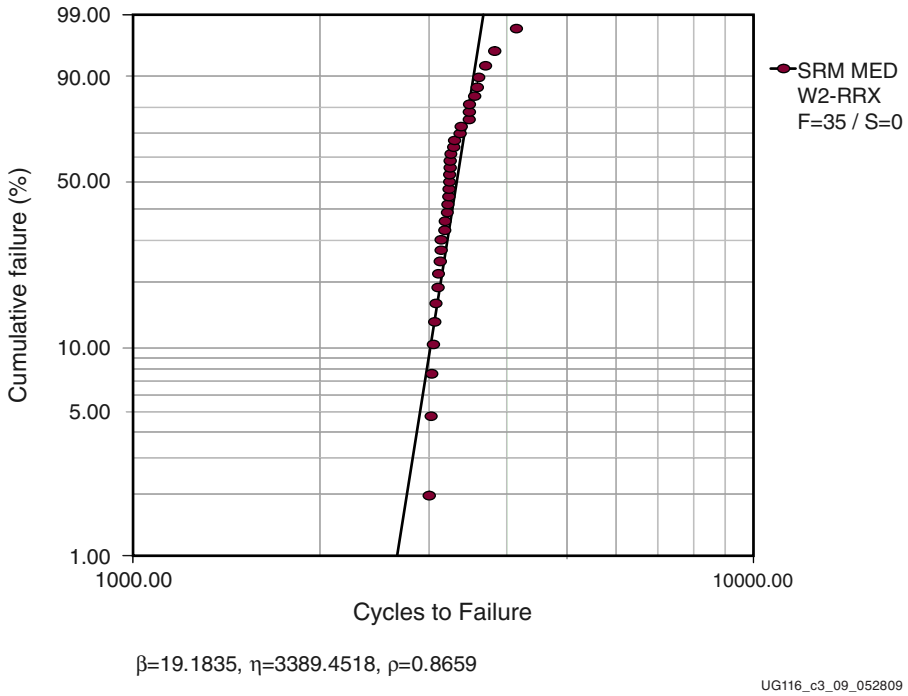

Figure 3-9: **Cycles to Failure in the Second-Level Reliability Tests for FF1704**

Board-Level Reliability Tests, Pb-Free

FGG676, FFG1152

Table 3-72: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FGG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FFG1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	23 x 23	1.152 thick 6-layer
FFG1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, OSP finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- FGG676: 0°C – 100°C, 40-minute thermal cycle, 10 minutes dwells, 10°C/minute ramp rate
- FFG1152: 0°C – 100°C, 10 minutes dwells, 5 minutes ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: resistance of net > threshold resistance (300Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-73: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FGG676	7,027	35	27	4,390	5,974
FFG1704	5,000	32	0	NA	NA
FFG1152	4,640	28	26	3,186	4,121

Weibull Plots

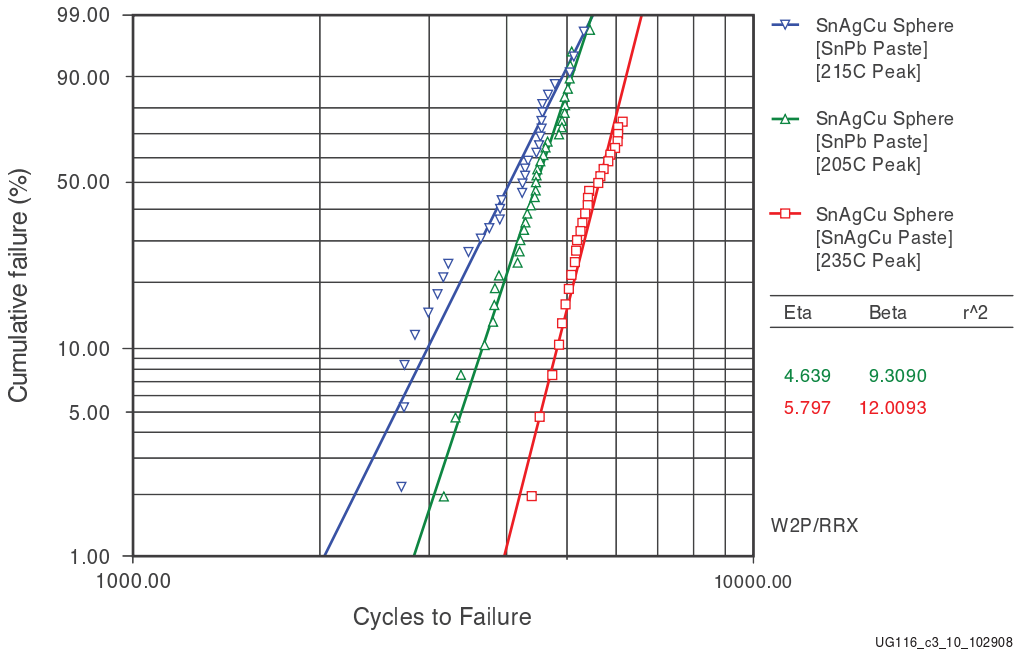

Figure 3-10: **Cycles to Failure in the Second-Level Reliability Tests for FGG676**

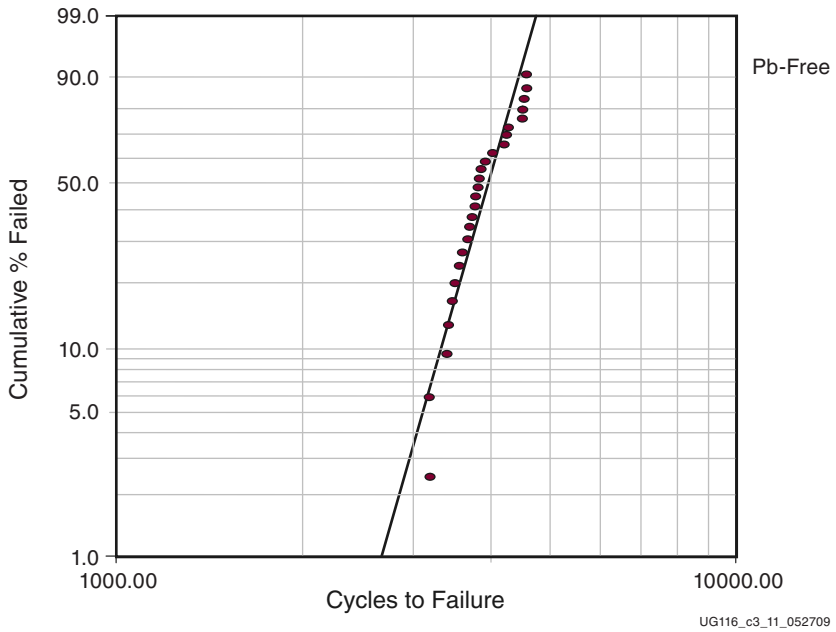

Figure 3-11: **Cycles to Failure in the Second-Level Reliability Tests for FFG1152**

FBG900

Table 3-74: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FBG900	31 X 31	900	1.00	0.60	0.53	SMD	12.93 x 16.91	0.95 thick, 8-layer

Mother Board Design and Assembly Details

FBG900

- 8-layer, FR-4, 220 x 140 x 2.36 mm size, ENIG finish
- 0.45 mm pad diameter/0.55 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- OPEN: resistance of net > threshold resistance (500Ω)
- FAIL: At least 2 opens within one cycle, log 15 failures for each net

Table 3-75: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FBG900	10085	32	18	5674	9148

Weibull Plots

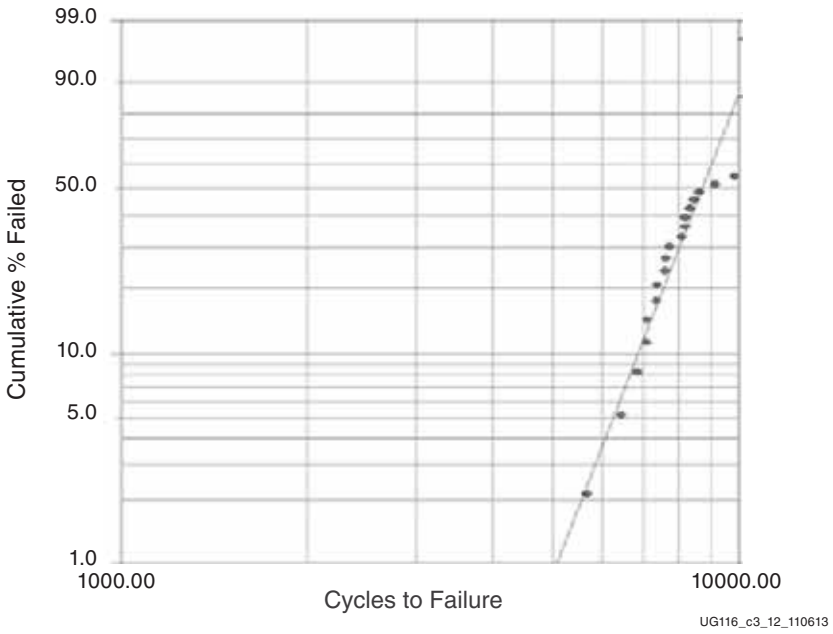

Figure 3-12: **Cycles to Failure in the Second-Level Reliability Tests for FBG900**

SBG484

Table 3-76: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
SBG484	19 X 19	484	1.00	0.50	0.40	SMD	10.82 x 12.04	0.98 thick 8-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.36 mm size, ENIG finish
- 0.33 mm pad diameter/0.50 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.

Test Condition

- 0°C - 100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- OPEN: resistance of net > threshold resistance (500Ω)
- FAIL: At least 2 opens within one cycle, log 15 failures for each net

Table 3-77: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SBG484	6827	32	23	4499	6608

Weibull Plots

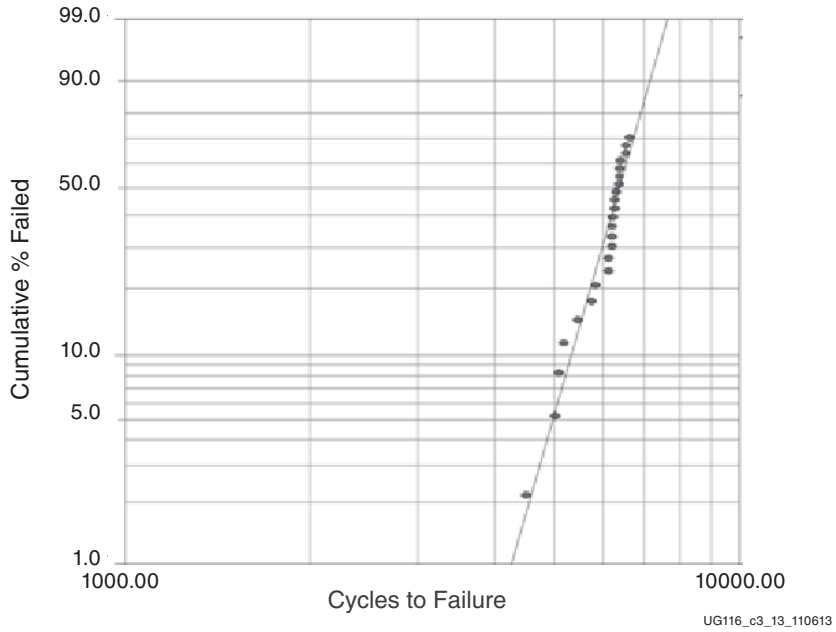

Figure 3-13: **Cycles to Failure in the Second-Level Reliability Tests for SBG484**

FFG1928

Table 3-78: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFG1928	45 X 45	1924	1.00	0.60	0.53	SMD	23.85 x 21.65	1.33 thick 12-layer

Mother Board Design and Assembly Details

- 16-layer, FR-4, 220 x 140 x 2.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: resistance of net > threshold resistance (500Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-79: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFG1928	9007	32	15	6861	9313

Weibull Plots

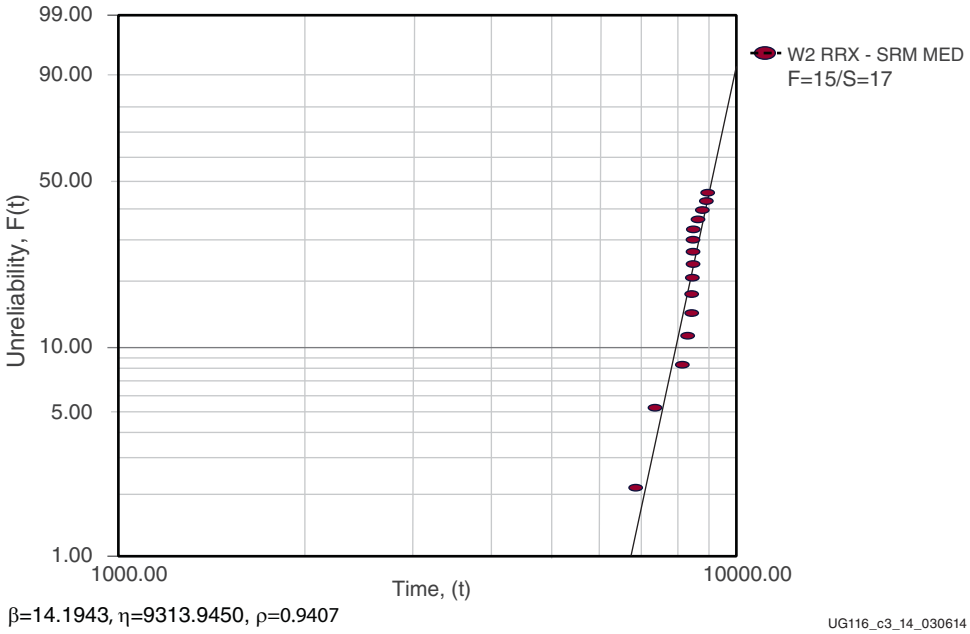

Figure 3-14: **Cycles to Failure in the Second-Level Reliability Tests for FFG1928**

FLG1925

Table 3-80: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FLG1925	45 X 45	1924	1.00	0.635	0.53	SMD	23.85 x 21.65	1.42 thick 12-layer

Mother Board Design and Assembly Details

- 16-layer, FR-4, 220 x 140 x 3.2 size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: resistance of net > threshold resistance (500Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-81: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FLG1925	6043	32	27	3789	5548

Weibull Plots

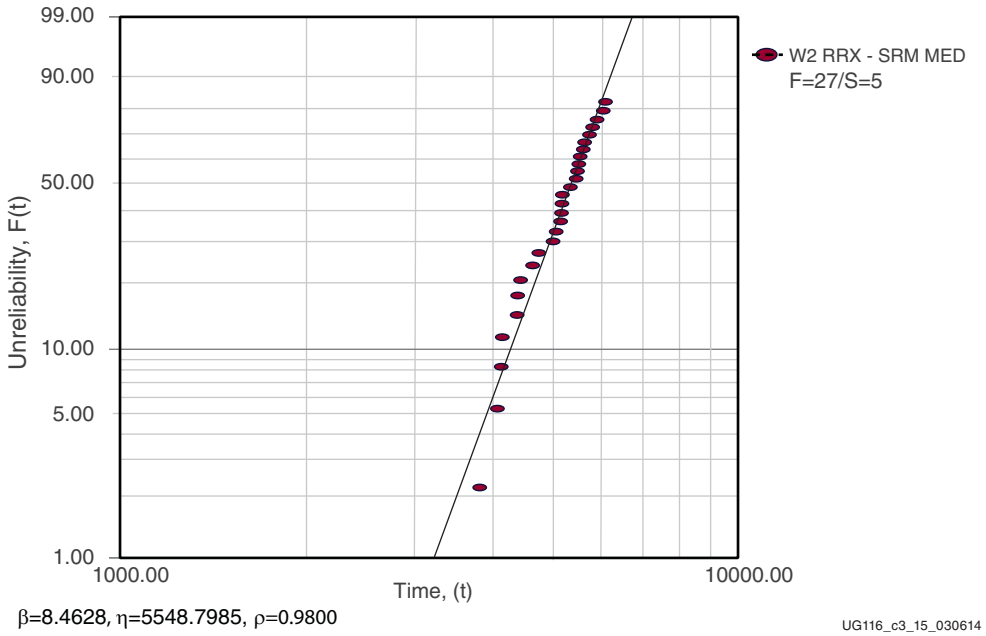

Figure 3-15: **Cycles to Failure in the Second-Level Reliability Tests for FLG1925**

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

1. *Device Package User Guide* (UG112)
2. *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* (WP286)

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